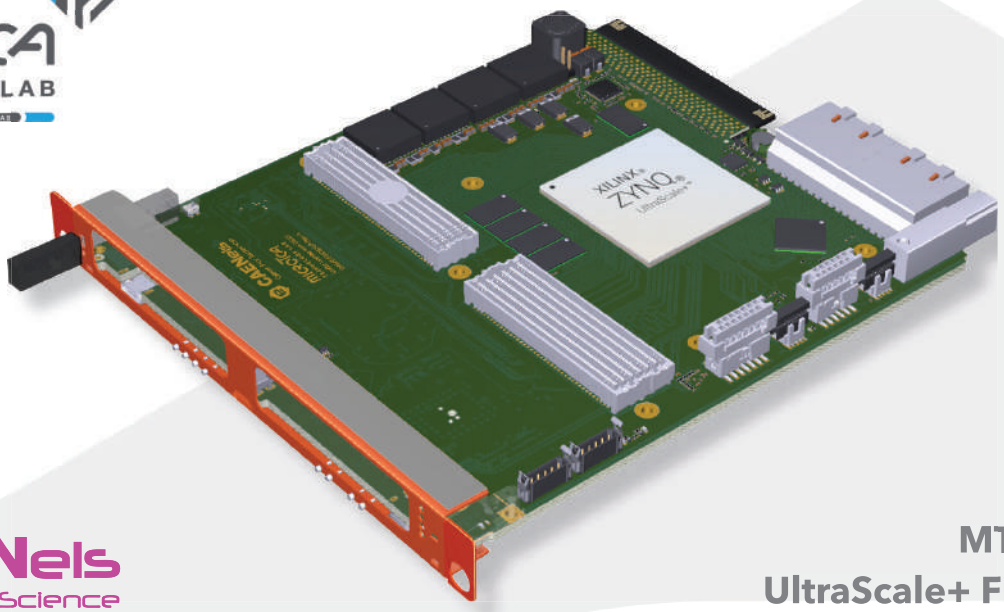
MICROTCA TECHNOLOGY LAB



CAENels Gear For Science

MTCA.4 ZYNQ UltraScale+ FMC+ Carrier

DAMC-FMC2ZUP

FEATURES

Recommended for **NEW DESIGNS**

- **FPGA Low-Power Xilinx UltraScale+ MPSoC XCZU11EG-L2FFVC1760E**
  - 653k Logic Cells, 2.928 DSP Slices, PCIe Gen. 4 x8, 100G Ethernet MAC
  - 1.5 GHz Quad-Core ARM Cortex-A53, MALI-400 GPU
  - 16 GTY transceivers (28.21 Gbps) routed to FMC+ transceivers
  - 32 GTH Transceivers (16.375 Gbps / 12.5 Gbps low-power) routed to FMC HPC, backplane, Front Panel, Zone3
  - 4 GTR Transceivers (6.0 Gbps) routed to SATA links and USB Type-C connector
  - 21.1 MB of BlockRAM, 22.5 MB of UltraRAM
  - C1760 package is compatible to ZU17EG (926k logic cells) and ZU19EG devices (1143k logic cells)
  - FPGA core voltage can be set to low-power (0.72V) or standard power operation via MMC user command allowing to switch between low-heat dissipation or highest transceiver performance
- **One FMC+ Slot with 24 transceivers connected (16 GTY + 8 GTH) - all LA and HA pins are connected**
- **One standard FMC HPC socket**
- **USB C-Type connector at the front panel that provides DisplayPort signals and USB 3.0 interface. This allows a stand-alone system with monitor output and USB host port saving a CPU module**
- **Zone3 Class D1.1 compliance with full interlock support**
- **64-bit 4 GB DDR4 with 2400 MT/s connected to PS - accessible from PL via AXI Bridge**
- **16-bit 1 GB DDR4 with 2666 MT/s (2400 MT/s in low-power mode) connected to PL**
- **Flexible clocking with capability to receive and drive all MTCA backplane clocks (TCLKA, TCLKB, TCLKC, TCLKD, FMC bidirectional clocks) and 3 PLLs to generate clocks for PS, Zone3 and FMC transceivers**
- **White Rabbit Support (input from front panel, output to backplane via M-LVDS and TCLKs)**
- **SD-Card slot (connected to PS) accessible via front panel**
- **8 GB eMMC Memory connected to PS**
- **Full MLVDS and interlock receive/drive capability**
- **JTAG support from on-board connector or AMC backplane (JSM module) with FPGAs, FMCs and RTM as targets**
- **Full HPM update functionality**
- Design is compatible with all FPGA speed grades

About Us

The MicroTCA Technology Lab is one of seven Innovation Labs funded by the Helmholtz Association. DESY together with partners has created this User Innovation Lab. Our goal is to foster the electronics standard MicroTCA in research and industry. We want to facilitate the use of MicroTCA and support new and existing users of the technology with our products and services.

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About Us

CAEN ELS is a leading company in the design of power supplies and state-of-the-art complete electronic systems for the Physics research world, having its main focus on dedicated solutions for the particle accelerator community and high-end industrial applications.

- Power Supply Systems
- Precision Current Measurements
- Beamline Electronic Instrumentation
- FMC and MicroTCA

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Front View

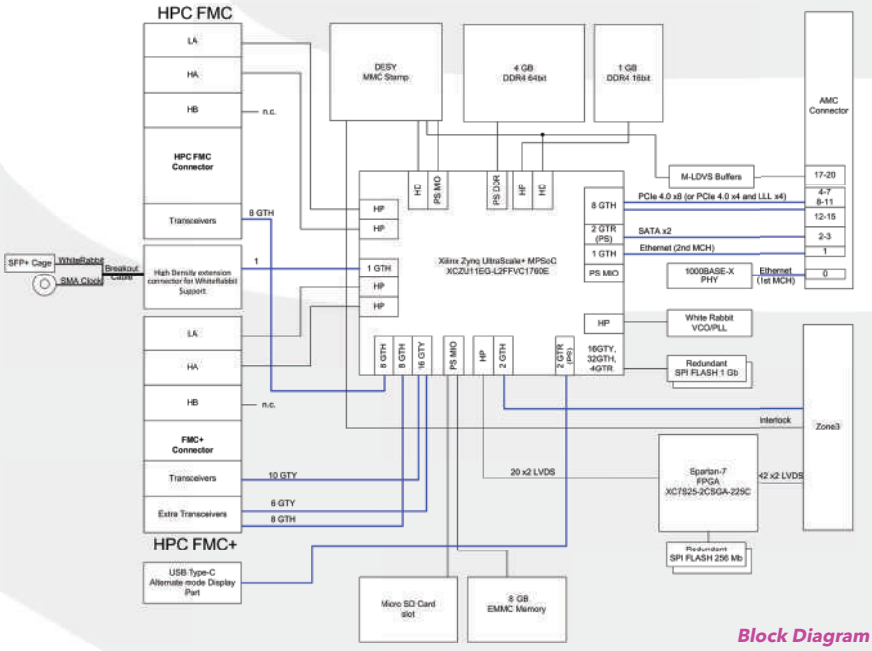
DAMC-FMC2ZUP is a high-end FMC+ carrier in MTCA.4 form factor based on the new ZYNQ UltraScale+ MPSoC. The FPGA on this carrier is the **Xilinx ZU11EG**. The programmable logic features 653k logic cells, 2920 DSP slices and 48 Multi-Gigabit Transceivers. The Programmable System is based on a quad-core **ARM Cortex-A53** operating at 1.5 GHz.

All MTCA.4 backplane ports are connected to the FPGA. PCI express (port 4-7 and 8-11) is supported in gen. 3.0 x8 configuration. The point-to-point MGT interface (low-latency link) can be used with 4 or 8 lanes width (when PCIe is used in x4 configuration). Gigabit Ethernet (port 0) is connected to Processing System (ARM) and provides convenient access for development and for running application servers. Eight M-LVDS Timing/Trigger signals and four TCLK lines are also connected. The board features two DDR4 memory interfaces with 64 bit/4GB connected to PS and 16/1GB bits connected to PL, operating at 2400 MT/s and 2666 MT/s respectively.

The board has two FMC sockets: 24 transceivers are routed to the FMC+ socket and can be operated at up to 28.21 Gbps. The other one has a standard HPC connector with 8 transceivers connected, capable of operating at up to 16.375 Gbps. All HA and LA lines are connected on both FMC slots.

The board also provides a front panel connector with Gigabit Ethernet interface (over a SFP+), clock input and two trigger in/out signals. The front panel Gigabit Ethernet connection can be also used as White Rabbit endpoint. A flexible clocking system with a 16-channel bi-directional cross point switch allows to receive all clocks from and drive all clocks to the backplane (TCLKA, TLCKB, TCLKC, TCLKD) and to and from the FMCs (bi-directional clocks). The RTM interface is designed according to class D1.1 and carries full 42 LVDS lines and 2 MGT links. The board can support all existing digital RTMs from DESY, such as DRTM-AD84, DRTM-VM2, DRTM-PZT4. The ARM Cortex-A53 processor in the MPSoC can run GNU/Linux from a MicroSD card on the front panel or from an embedded 8GB eMMC. The Processing System is equipped with an USB Type-C interface at the front panel that supports alternate mode. The alternate mode allows to connect to a Display and provides an USB 3.0 interface at the same time, providing the possibility to omit CPU boards in MTCA systems. Two transceivers from PS are connected to AMC port 2 and 3, allowing attachment of up to two standard off-the-shelf MicroTCA SATA cards with hard drives or SSDs.

Being supported by all modern development tools by Xilinx, such as Vivado, HLS, Yocto, Petalinux, SDSoC and SDAccel, DAMC-FMC2ZUP is a board capable of addressing ever-growing needs in terms of processing power, while also reducing development time. Combination of a large FPGA and a powerful CPU provides extreme flexibility required by a general-purpose FMC carrier.



Block Diagram

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