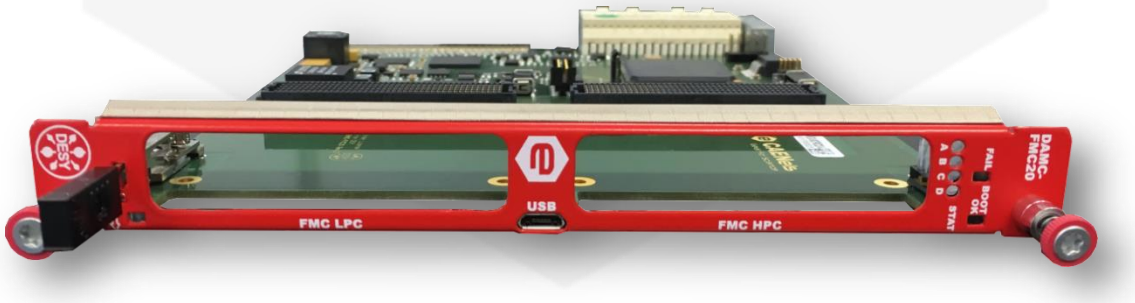
DAMC-FMC20

Dual FMC
Carrier Board with
MTCA.4 REAR I/O

CAENels
Gear For Science

User's Manual



MTCA.4 – MicroTCA for Physics

Rev. 1.0 – June 2019

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Document Revisions

Document Revision	Date	Comment
1.0	June 25th, 2019	First Release

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CAUTION

- This instrument is designed for indoor use and in area with low condensation.

The following table shows the general environmental requirements for a correct operation of the instrument:

Environmental Conditions	Requirements
Operating Temperature	0°C to 50°C
Operating Humidity	30% to 85% RH (non-condensing)
Storage Temperature	-10°C to 60°C
Storage Humidity	5% to 90% RH (non-condensing)

This manual refers to the following boards:

- **DAMCFMC20XAA** - Dual FMC Carrier Board - MTCA.4 - Dual-FPGA Processing

1. Introduction

This chapter describes the general characteristics and main features of the DAMC-FMC20 board.

1.1 DAMC-FMC20 Description

The DAMC-FMC20 is a cost-efficient FPGA mezzanine card (FMC) carrier designed according to MTCA.4, it is equipped with two Spartan-6 FPGAs and it simultaneously supports one low pin count and one high pin count FMC module.

While one FPGA allows serial high-speed communication (PCIe, RTM, Backplane, FMCs), the other one allows implementing large signal processing algorithms. The carrier supports one serial link (GTP) for HPC FMC module and up to two serial links for LPC FMC module.

In addition, an extra 12V power connector for high current FMC applications is foreseen for each FMC module.

The carrier provides one PCIe link that is AMC.1 type 1 compliant; the carrier is also software-reconfigurable over PCIe and MMC. The AMC ports 12-15 are connected via cross-point switch to the transceiver FPGA.

The board is a cost-effective approach for basic IO without high-demanding computing requirements; an additional USB connection is optional for direct debugging the FPGAs and MMC at the front panel.

The carrier management is compliant to the latest recommendation MMC V1.0. The carrier Zone 3 is compliant to the Class D1.0.

The board provides the following features:

- Double width, mid-size MTCA.4 form factor Advanced Mezzanine Card (AMC)
- Dual-FPGA processing
- Xilinx XC6SLX45T for serial communication including PCIe (transceiver FPGA)

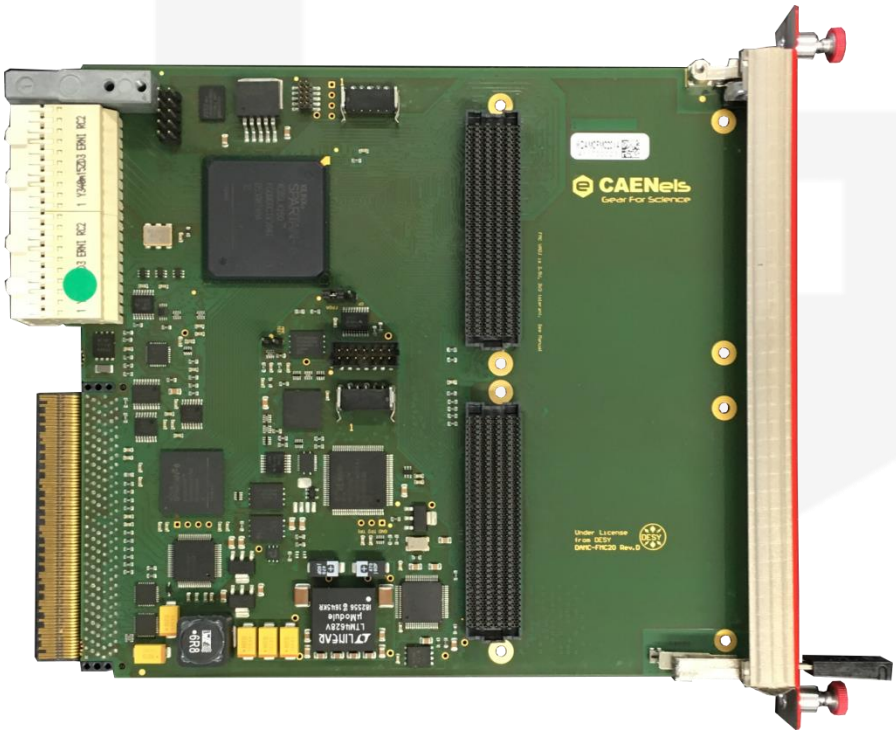
- Xilinx XC6SLX150 for signal processing and connectivity to RTM and FMCs (main FPGA)
- Rear IO connected to FPGA, Class D1.0 compatible
- Supports 2 FMCs: One HPC module and one LPC module
- Front panel with hot-plug switch, mandatory LEDs required by IPMI standard and four additional LEDs
- USB debug interface at front panel for FPGAs and MMC controller
- Remote configurable over PCIe, MMC or download cable
- ANSI/VITA 57.1 compliant
- Extra power connector for booth FMCs
- IPMI 1.1 compliant MMC
- RoHS compliant

1.2 DAMC-FMC20 Overview

The DAMC-FMC20 main components are listed in the below table:

Component	*Purpose*	*Manufacturer*
XC6SLX150-3FG900I	**Main FPGA**	**Xilinx**
XC6SLX45T-2CSG324I	**Transceiver FPGA (PCIe bridge and MGT)**	**Xilinx**
SN65LVCP408	**8x8 crosspoint switch**	**Texas Instruments**
ICS874003	**PCIe jitter attenuator**	**Intersil**
FT4232H	**Hi-speed quad USB UART IC**	**FTDI**
ATxmega128A1	**MMC controller**	**Atmel**
TPS2458	**Hotswap controller, load current monitor**	**Texas Instruments**

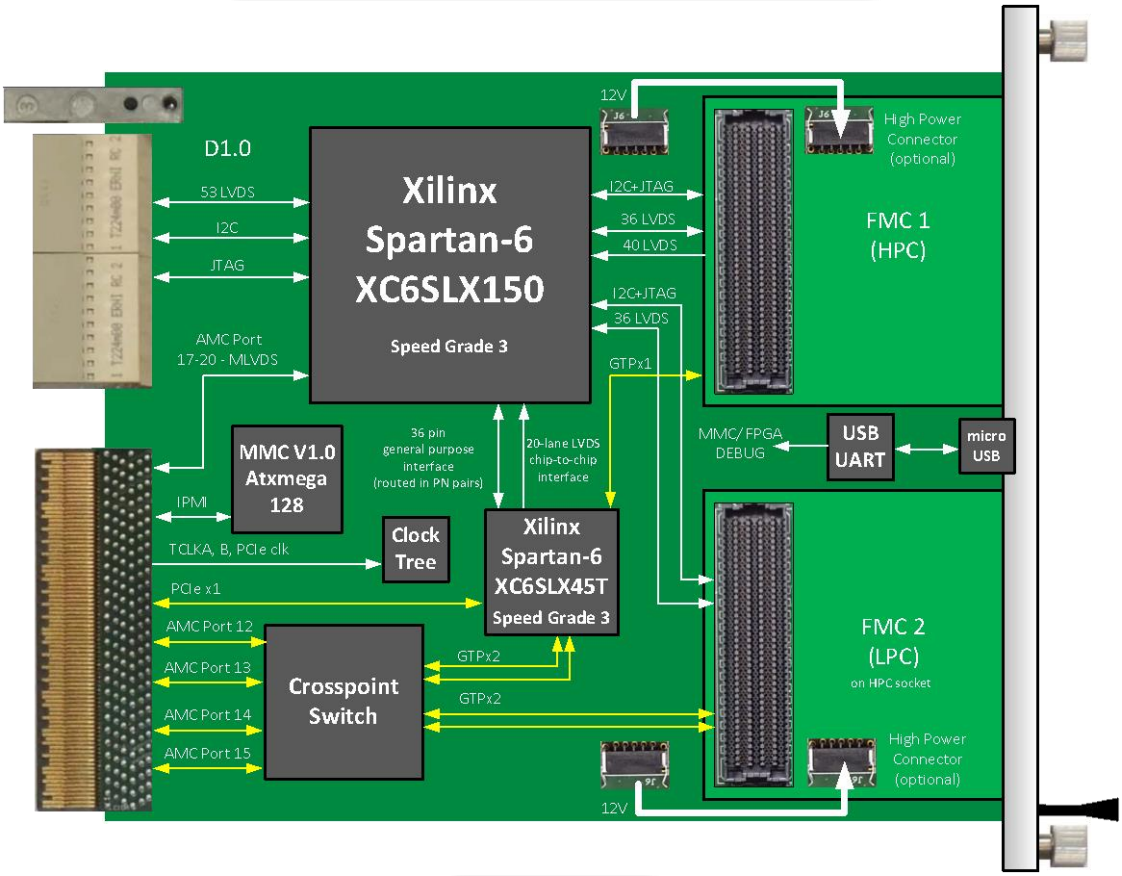
Such components are placed on the board as in the picture below:



1 *Main FPGA XC6SLX150*
2 *HPC FMC power output connector*
3 *LPC FMC power output connector*
4 *JTAG connector*
5 *FMC HPC connector*
6 *FMC LPC connector*
7 *USB connector*
8 *AMC connector*
9 *Transceiver FPGA XC6LX45T*
10 *Cross-point switch*
11 *MMC ATxmega128A1*
12 *2 SPI FLASH ICs*
13 *XC6LX150 Platform FLASH*
14 *RTM connector*

2. DAMC-FMC20 Architecture

In this chapter a deep technical overview of the DAMC-FMC 20 board is given; the basic block diagram is presented below:



The transceiver FPGA provides control over PCIe and processes all serial links. It is connected to the main FPGA through a 64 bit parallel chip-to-chip interface; furthermore, both FPGAs are connected via four LVDS lanes.

Note that Xilinx Spartan only supports LVDS driver on Bank 0 and on Bank 2, this limiting the number of pins that are available for bidirectional LVDS communication. DAMC-FMC20 pin assignment allows all LVDS pins on RTM and full bidirectional LVDS on LPC.

On HPC FMC, while the LPC pins (36 lanes) can operate in bidirectional mode, the additional HPC pins (40 lanes) are input-only LVDS.

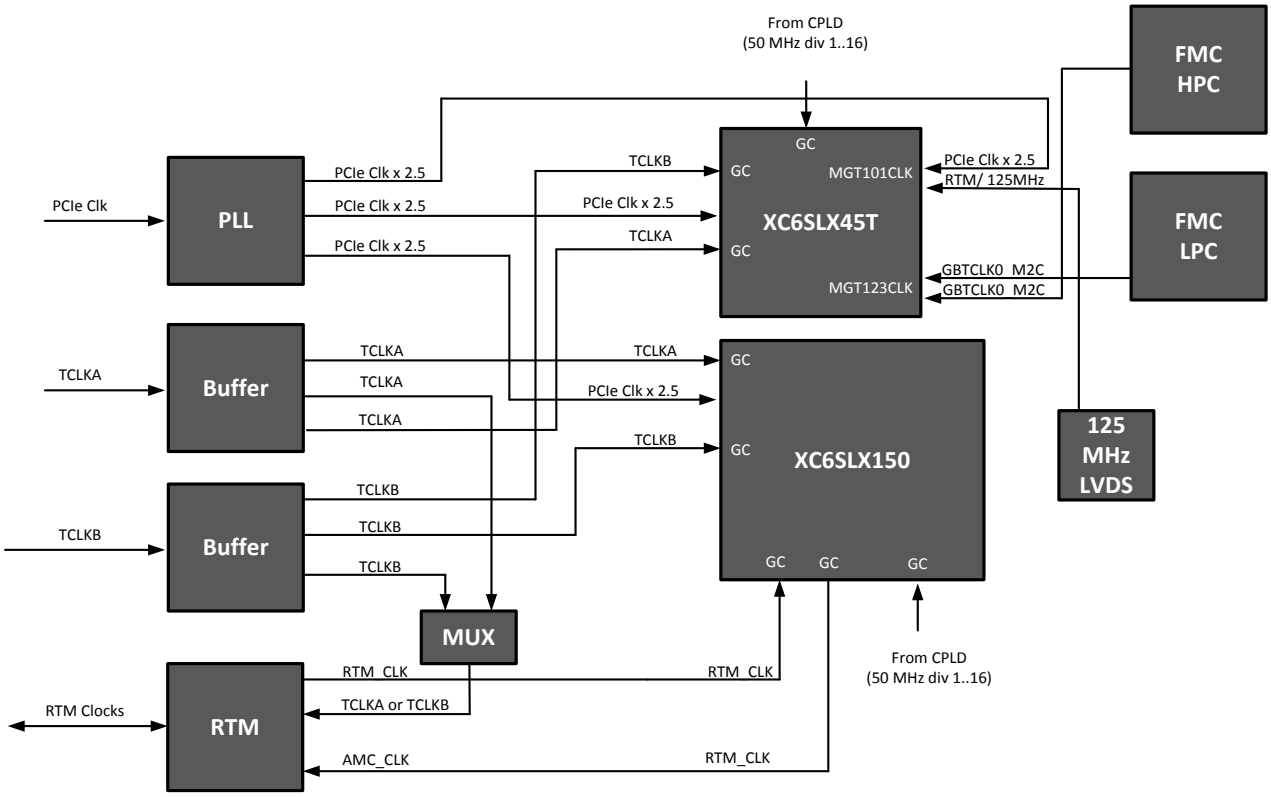
If outputs on these pins are desired, other standards such as LVCMOS25 must be used.

2.1 Clock Tree

The DAMC-FMC20 has a flexible clock tree, since FPGA global clocks can be accessed from PCIe clock as well as from TCLKA or TCLKB. Furthermore, local 200 MHz oscillators are present for booth FPGAs.

A clock from RTM is fed to the main FPGA and to the transceiver FPGA. A multiplexer selects if TCLKA or TCLKB are output to RTM.

The clock tree diagram is presented below:



The clock tree provides following features:

- Distribution of PCI clock (multiplied by factor 2.5) to transceiver FPGA GTP block, transceiver FPGA global clock and main FPGA global clock;
- Distribution of TCLKA to transceiver FPGA global clock, main FPGA global clock and RTM (multiplexed with TCLKB);

- Distribution of TCLKB to main FPGA global clock and RTM (multiplexed with TCLKA);
- Distribution of RTM clock to main FPGA global clock and transceiver FPGA (MGT clock);
- Two clock sources for first MGT tile on transceiver FPGA: PCIe clock and FMC clock;
- Two clock sources for second MGT tile on transceiver FPGA: FMC clock and (as a placement option) RTM clock or 125 MHz fixed LVDS clock;
- 200 MHz LVDS clock source for each FPGA as global clock.

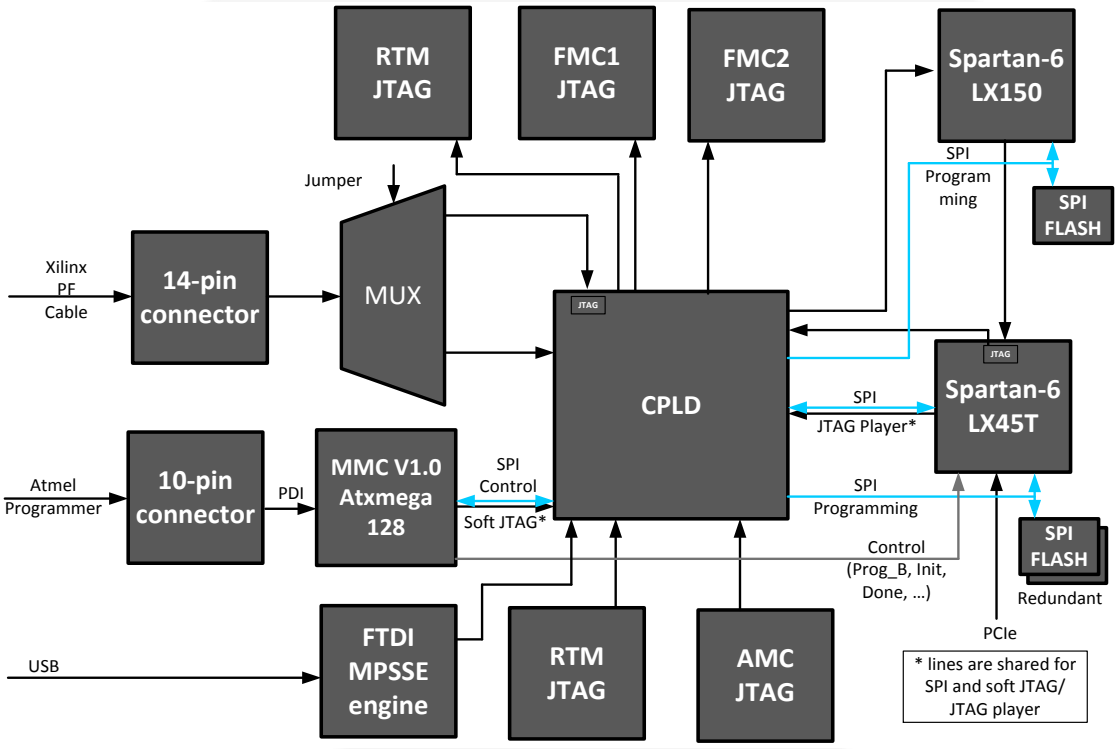
2.2 JTAG Chain

The DAMC-FMC20 is provided with a high-flexibility JTAG chain, which can be routed to Xilinx Platform Cable connector, Soft-JTAG over USB (FTDI MPSSE) or AMC connector.

A CPLD that is controlled over MMC's IPMI or over MMCs UART debug interface (over USB) selects the configuration of the chain, which contains the transceiver FPGA by default.

Optionally, main FPGA with dedicated Platform FLASH, RTM and/ or booth FMCs can be included in the chain.

Below a schematic of the chain is presented:



The chain provides following features:

- JTAG input from 14-pin connector, AMC, soft JTAG player (in MMC or transceiver FPGA);
- JTAG output to transceiver FPGA and main FPGA (including Platform FLASH);
- Extended JTAG output to RTM, FMC1 and FMC2;
- Controlled over Xilinx CoolRunner-II CPLD (code based on DESY MMC V1.0 reference design);
- JTAG chain configuration over IPMI interface on MMC or over UART interface on MMC.

2.3 FLASH Programming

Following ways exist to program the on-board FLASH memories:

MMC Atmel ATxmega 128A1 (integrated FLASH memory)

- Programming with programming cable using 6-pin Atmel PDI connector;
- In-crate programming using HPM1.*

FPGAs (2 SPI FLASH memories)

- Programming using Xilinx Platform Cable;
- Programming over AMC backplane or USB* (MPSSE);
- Programming over PCIe-to-SPI Interface (supported by Reference BSP);
- Direct SPI Programming over IPMI (programming of 2 images; supported by MMC V1.0 reference code).

RTM, FMC1, FMC2

- Programming using programmer on 14-pin connector;
- Programming over AMC backplane or USB* (MPSSE);
- Programming using JTAG player in transceiver FPGA;
- Programming over JTAG player* in MMC.

* *software support not included yet*

2.4 Module Management

The MMC is implemented in an ATxmega128A1 microcontroller. The IPMI protocol is compliant to IPMI 1.1 standard, RTM and FMCs have separate I2C connections to the microcontroller.

The MMC has an additional EEPROM for configuration purposes and a temperature sensor for measuring the cooling performance in the uTCA crate. The

hot-plug switch and LEDs required by IPMI standard are present, while an optional USB connector is present at the front panel for debugging the controller.

The programming of the microcontroller is done through a direct SPI connection or the common JTAG chain of the board.

2.4.1 On-board Diagnostics

The board contains an optional FT4232 four-channel USB bridge chip, and the two Xilinx FPGAs, the MMC and the JTAG interface are connected to each of its channels for debugging and monitoring. A temperature sensor and monitoring capability of all supply voltages is implemented in the MMC using ADCs, while four LEDs at the front panel show user defined status of the FPGAs.

2.4.2 On-board Voltage Monitoring and Implemented Functions

The DAMC-FMC20 follows the MMC V1.0 recommendation, following voltages can be monitored:

- Monitoring of 1.2V GTP;
- 1.2V FPGA core voltage (main and transceiver FPGA);
- 1.8V monitoring;
- 2.5V monitoring;
- 3.3V monitoring;
- 3.3V management power monitoring;
- 12V payload power monitoring;
- RTM power and current measurement: Power to RTM Interface (12V and 3V3) is controlled by MMC via dedicated power switch. Current consumption is monitored via ATxmega analog inputs).

The following functions are supported:

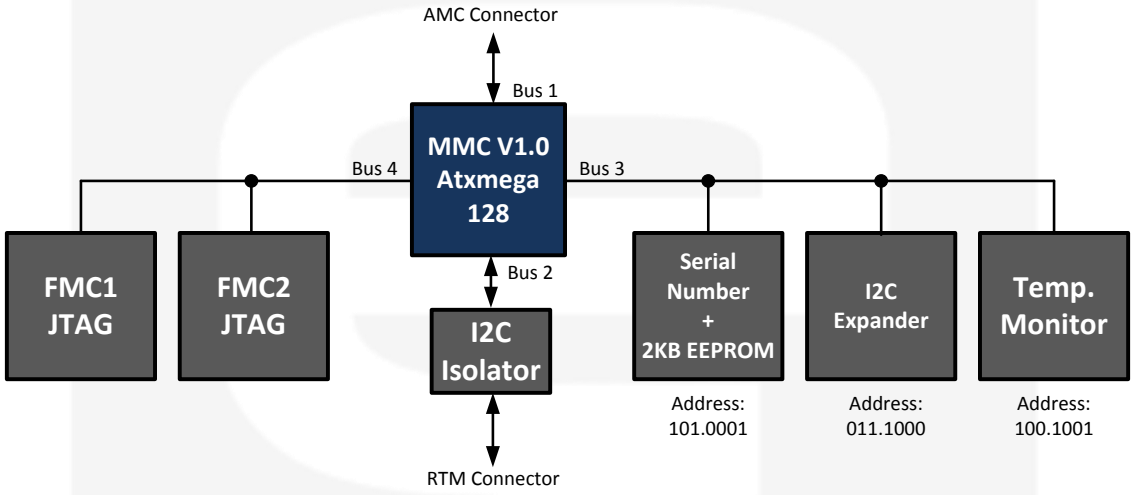
- Hot-swap handle control;
- Regulator power good monitoring;
- FMC power good monitoring;
- FMC present monitoring;

- UART debug interface (over UART-to-USB translator);
- Transceiver FPGA SPI FLASH programming (2 memories);
- Transceiver FPGA control (reset, reboot etc.).

2.4.3 I2C Buses

MMC on DAMC-FMC20 has four independent I2C buses: Bus one is connected to the AMC interface (IPMI-B), Bus two is connected to the RTM using an I2C isolator and Bus three is connected to on-board sensors. Addresses are: 0x51 for serial number IC, 0x38 for I2C expander and 0x49 for temperature monitor.

A schematic is presented below:



2.4.1 AMC Connectivity

Available connections are presented in the below table:

Channel	*Signal*	*Voltage levels*	*Protocol/Signal*	*Remarks*
4	**PCIe x1 (lane 0)**	**CML**	**AMC.1**	**PCIe Bus**
12	**cross point switch**	**CML**	**custom**	**RIO (Xilinx)**
13	**cross point switch**	**CML**	**custom**	**RIO (Xilinx)**
14	**cross point switch**	**CML**	**custom**	**RIO (Xilinx)**

15	cross point switch	CML	custom	RIO (Xilinx)
17_RxD	TRGSTART	MLVDS	custom	bidirectional
17_TxD	TRGEND	MLVDS	custom	bidirectional
18_RxD	TRGREADOUT	MLVDS	custom	bidirectional
18_TxD	CLK_AUX	MLVDS	custom	bidirectional
19_RxD	RESET	MLVDS	custom	bidirectional
19_TxD	INTERLOCK0	MLVDS	custom	bidirectional
20_RxD	INTERLOCK1	MLVDS	custom	bidirectional
20_TxD	INTERLOCK2	MLVDS	custom	bidirectional
TCLKA	f = 108 MHz	LVDS - terminated	fast clk	input
TCLKB	f = 4.514 MHz	LVDS - terminated	slow clk	input
FCLKA	f = 100 MHz	LVDS	sclock for PCIe	input
JTAG	JTAG	LVCMOS (3.3 V)	JTAG chain	
IPMI	IPMI	LVCMOS (3.3 V)	IPMI for MMC (SCL/SDA)	with pull-up
PS	PS0, PS1	LVCMOS (3.3 V)	presence detect	with pull-up
GA	GA0/GA1/GA2	LVCMOS (3.3 V)	geographical address	pull-up by MMC
Enable_n	Enable_n	LVCMOS (3.3 V)	enable	with pull-up
MP +3V3	MP +3V3	Power supply	management power	0,15 A/150 uF
PP +12V	PP +12V	Power supply	payload power	7,4 A/800 uF

2.5 RTM Connector

The Z3 RTM connector carries following electrical signals (according to Class D1.0):

- AMC clock (global clock from main FPGA going to AMC)
- TCLKA or TCLKB (clock from AMC to RTM)
- RTM present signal
- RTM I2C (isolated, control from MMC)
- RTM clock (clock from RTM going to AMC)
- JTAG interface (connected to CPLD)
- Bidirectional LVDS bus (connected to 2.5V FPGA bank)

- 3V3 management power (switched through MMC)
- 12V payload power (switched through MMC)

2.5.1 Zone 3 Class Compatibility

The connector is compatible to the double row B+ connector specified in Advanced Mezzanine Card Base Specification; the connectivity of signals is based on the PICMG MTCA.4 RI.0 draft 0.7d specification (Revision 1.0 Draft 0.1p4).

The Zone 3 connector (J30) is compliant to Class D1.0 (54 LVDS I/O signals; LVDS 2.5V). All IO lines are connected to differential IO pins of the XC6SLX150 Spartan-6 FPGA as reported in the tables below:

		a	b	c	d	e	f
1		PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2		PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS
3		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
4		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
5		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
6		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
7		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
8		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
9		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
10		P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO

Table 1: AMC Z3 J30 pin assignment for Class D1.0

		a	b	c	d	e	f
1		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
2		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
3		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
4		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
5		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
6		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
7		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
8		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
9		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
10		P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-

Table 2: AMC Z3 J31 pin assignment for Class D1.0

2.6 FMC Connectors

The board provides one LPC and one HPC FMC connector. The LPC provides following features:

- Two serial links with speeds of 2.7Gbps or 3.2Gbps, depending on speed grade of the transceiver FPGA;
- One LVDS clock pair (module to carrier) that is connected to main FPGA global clock input;
- JTAG interface connected to CPLD.

2.6.1 FMC Connectors Remarks

The FMC adjustable voltage VADJ is fixed to 2.5V and all FMC signals are connected to a 2.5V bank to support LVDS and LVCMOS25 standards.

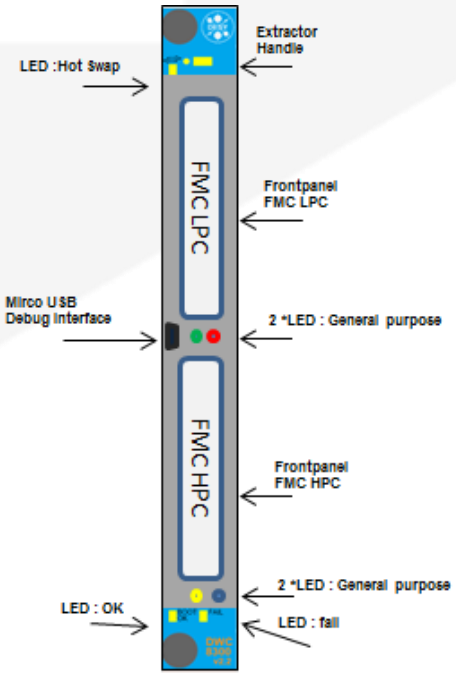
For Spartan-6, the maximum input voltage on all input pins is 4.1V for LVCMOS25, while Spartan-6 minimum output voltage on 2.5V bank is 2.1V. These levels allow compatibility to many 3.3-V ICs (LVCMOS33).

Additional details can be found in the Xilinx document "Spartan-6 DC and Switching Characteristics".

2.7 LED Indicators

The board provides following LED indicators:

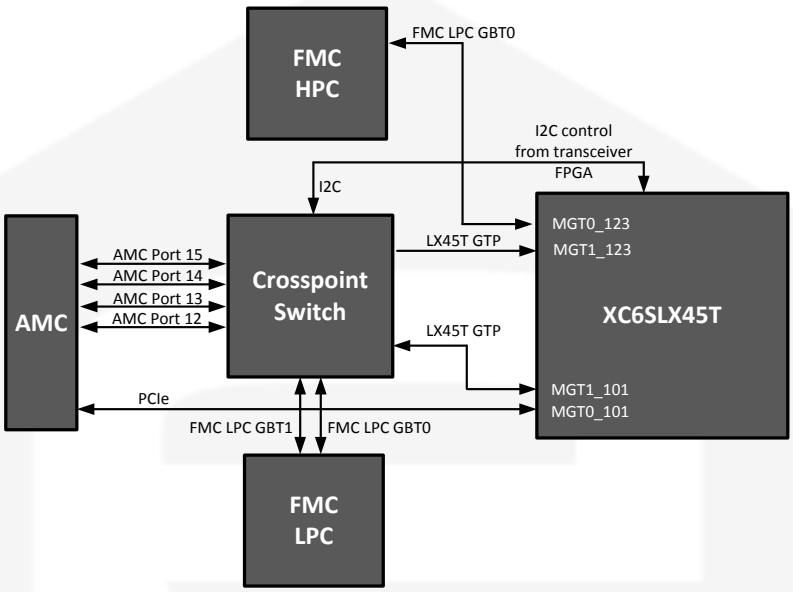
- One green LED per FMC channel (FPGA controlled);
- One yellow LED per FMC channel (FPGA controlled);
- One red/green bi-color LED controlled by MMC;
- One blue LED controlled by MMC (management state indication).



2.8 MGT Routing and Crosspoint Switch

MGTs are available on transceiver FPGA; the XC6SLX45T contains two dual MGTs providing four serial transceivers in total.

One transceiver (MGT0_101) is fixed to PCIe, while the second transceiver (MGT0_123) is fixed to FMC HPC; in addition, two transceivers are routed to cross-point switch. These transceivers can be individually routed to AMC Ports 12 to 15 or FMC LPC:



The cross-point switch provides routing of MGT lanes to AMC and LPC connectors as described in the table below:

Signal Name	Channel In	Channel Out	Signal Name
AMC_RX15	0	7	AMC_TX12
AMC_RX14	1	6	AMC_TX13
AMC_RX13	2	5	AMC_TX14
AMC_RX12	3	4	AMC_TX15
NC	4	3	NC
NC	5	2	NC
NC	6	1	MGT1_101 RX
MGT1_101 TX	7	0	NC

2.9 Power Supply Architecture

While the board needs multiple supply voltages, all these voltages are generated from the 12V power of the AMC connector.

All supply voltages can be monitored over IPMI. In the special case of programming the MMC controller the first time, the 3.3V management power can be delivered by the SPI programmer on the SPI download connector, in this way being possible to program the MMC outside the crate without additional power supply.

Power domains are listed below:

Power Domain	Source
12V for RTM	over hot-swap controller from AMC connector
3v3 MP for RTM	over hot-swap controller from AMC connector
12V for FMCs	direct from AMC Power
3V3 for FMCs	common 3V3 switching regulator 10A
2v5 for FMCs	common 2V5 switching regulator 10A
2v5 for Xilinx IO Power	common 2V5 switching regulator 10A
1v8 for EEPROMS	linear regulator from 3V3
1v2 for Xlilinx XC6SLX150	dedicated 1.5A linear regulator
1v2 for Xlilinx XC6SLX45T	dedicated 0.5A linear regulator
1v2 for MGT Links	dedicated 0.5A linear regulator
3V3 MP for MMC	direct from AMC connector or SPI programmer
12V extra Power for FMC	direct from AMC Power

2.10 Connector Pin Assignments

The board contains a 160-pin female connector by Samtec, type ASP-134603-01, for the LPC and a 400-pin female connector by Samtec, type ASP-134486-0,1 for the HPC FMC mezzanine card.

The optional debug interface uses a Micro USB connector type B (Molex 47346-0001). The Xilinx programmer is connected through a 14-pin miniGrid connector type Molex 87832-1420. The SPI interface uses a standard 6-pin 2.54-mm rectangular connector.

2.10.1 FMC Power Connector

Please note that one additional connector is available in order to supply more power (up to 1.8 A per channel) with respect to the FMC standard (specified at 1A for to the module). The connector provides 12V, identical to the power available at FMC connector.

Pin assignment of on-board 12V power connector is provided below:

Pin number	Connection
1	12V
2	GND
3	12V
4	GND
5	12V

2.10.2 JTAG Connector

Standard Xilinx Platform Cable Connector (MOLEX – 87832-1420) is used for JTAG connection as in the below table:

Pin No.	Net	Net	Pin No.
1	GND	NC	2
3	GND	NC	4
5	GND	TDI	6
7	GND	TDO	8
9	GND	TCK	10
11	GND	TMS	12
13	NC	VREF (3V3)	14

2.10.3 Atmel Programmer Connector

Standard Atmel PDI connector (standard 6 pin header) is used on DAMC-FMC20, which pinout is presented below:

Pin No.	Net	Net	Pin No.
1	PDI_DATA	3V3MP	2
3	NC	NC	4
5	RST	GND	6

2.10.4 RTM connector

J30 assignment is presented in the below tables:

No.	Name	Conn.
1a	12V	Switch
1b	12V	Switch
2a	12V	Switch
2b	12V	Switch
3a	AMC_CLK_P	FPGA
3b	AMC_CLK_N	FPGA
4a	TCLKA_P	Buffer
4b	TCLKA_N	Buffer
5a	RTM_D2_P	FPGA
5b	RTM_D2_N	FPGA
6a	RTM_D3_P	FPGA
6b	RTM_D3_N	FPGA
7a	RTM_D4_P	FPGA
7b	RTM_D4_N	FPGA
8a	RTM_D5_P	FPGA
8b	RTM_D5_N	FPGA
9a	RTM_D6_P	FPGA
9b	RTM_D6_N	FPGA
10a	RTM_D7_P	FPGA
10b	RTM_D7_N	FPGA

No.	Name	Conn.
1c	RTM_PS	MMC
1d	RTM_SDA	MMC
2c	3V3	Switch
2d	RTM_SCL	MMC
3c	RTM_CLK_P	FPGA
3d	RTM_CLK_N	FPGA
4c	RTM_D9_P	FPGA
4d	RTM_D9_N	FPGA
5c	RTM_D10_P	FPGA
5d	RTM_D10_N	FPGA
6c	RTM_D11_P	FPGA
6d	RTM_D11_N	FPGA
7c	RTM_D12_P	FPGA
7d	RTM_D12_N	FPGA
8c	RTM_D13_P	FPGA
8d	RTM_D13_N	FPGA
9c	RTM_D14_P	FPGA
9d	RTM_D14_N	FPGA
10c	RTM_D15_P	FPGA
10d	RTM_D15_N	FPGA

No.	Name	Conn.
1e	RTM_TCK	CPLD
1f	RTM_TDO	CPLD
2e	RTM_TDI	CPLD
2f	RTM_TMS	CPLD
3e	RTM_D16_P	FPGA
3f	RTM_D16_N	FPGA
4e	RTM_D17_P	FPGA
4f	RTM_D17_N	FPGA
5e	RTM_D18_P	FPGA
5f	RTM_D18_N	FPGA
6e	RTM_D19_P	FPGA
6f	RTM_D19_N	FPGA
7e	RTM_D20_P	FPGA
7f	RTM_D20_N	FPGA
8e	RTM_D21_P	FPGA
8f	RTM_D21_N	FPGA
9e	RTM_D22_P	FPGA
9f	RTM_D22_N	FPGA
10e	RTM_D23_P	FPGA
10f	RTM_D23_N	FPGA

J31 assignment is presented in the below tables:

No.	Name	Conn.
1a	RTM_D24_P	FPGA
1b	RTM_D24_N	FPGA
2a	RTM_D25_P	FPGA
2b	RTM_D25_N	FPGA
3a	RTM_D26_P	FPGA
3b	RTM_D26_N	FPGA
4a	RTM_D27_P	FPGA
4b	RTM_D27_N	FPGA
5a	RTM_D28_P	FPGA
5b	RTM_D28_N	FPGA
6a	RTM_D29_P	FPGA
6b	RTM_D29_N	FPGA
7a	RTM_D30_P	FPGA
7b	RTM_D30_N	FPGA
8a	RTM_D31_P	FPGA
8b	RTM_D31_N	FPGA
9a	RTM_D32_P	FPGA
9b	RTM_D32_N	FPGA
10a	RTM_D33_P	FPGA
10b	RTM_D33_N	FPGA

No.	Name	Conn.
1c	RTM_D34_P	FPGA
1d	RTM_D34_N	FPGA
2c	RTM_D35_P	FPGA
2d	RTM_D35_N	FPGA
3c	RTM_D36_P	FPGA
3d	RTM_D36_N	FPGA
4c	RTM_D37_P	FPGA
4d	RTM_D37_N	FPGA
5c	RTM_D38_P	FPGA
5d	RTM_D38_N	FPGA
6c	RTM_D39_P	FPGA
6d	RTM_D39_N	FPGA
7c	RTM_D40_P	FPGA
7d	RTM_D40_N	FPGA
8c	RTM_D41_P	FPGA
8d	RTM_D41_N	FPGA
9c	RTM_D42_P	FPGA
9d	RTM_D42_N	FPGA
10c	RTM_D43_P	FPGA
10d	RTM_D43_N	FPGA

No.	Name	Conn.
1e	RTM_D44_P	FPGA
1f	RTM_D44_N	FPGA
2e	RTM_D45_P	FPGA
2f	RTM_D45_N	FPGA
3e	RTM_D46_P	FPGA
3f	RTM_D46_N	FPGA
4e	RTM_D47_P	FPGA
4f	RTM_D47_N	FPGA
5e	RTM_D48_P	FPGA
5f	RTM_D48_N	FPGA
6e	RTM_D49_P	FPGA
6f	RTM_D49_N	FPGA
7e	RTM_D50_P	FPGA
7f	RTM_D50_N	FPGA
8e	RTM_D51_P	FPGA
8f	RTM_D51_N	FPGA
9e	RTM_D52_P	FPGA
9f	RTM_D52_N	FPGA
10e	RTM_D53_P	FPGA
10f	RTM_D53_N	FPGA

2.10.5 AMC Connector Pin Assignment

Presented in the below tables:

No.	Name	Conn.
1	GND	GND
2	PWR	+12V
3	PS1#	MMC
4	MP	+3V3
5	GA0	MMC
6	RSRVD	-
7	GND	GND
8	RSRVD	-
9	PWR	+12V
10	GND	-
11	TX0+	-
12	TX0-	-
13	GND	GND
14	RX0+	-
15	RX0-	-
16	GND	GND
17	GA1	MMC
18	PWR	+12V
19	GND	GND
20	TX1+	-
21	TX1-	-
22	GND	GND
23	RX1+	-
24	RX1-	-
25	GND	GND
26	GA2	MMC
27	PWR	+12V
28	GND	GND
29	TX2+	-
30	TX2-	-
31	GND	GND
32	RX2+	-
33	RX2-	-
34	GND	GND
35	TX3+	100R
36	TX3-	100R
37	GND	-
38	RX3+	100R
39	RX3-	100R
40	GND	-
41	ENABLE#	MMC
42	PWR	+12V

No.	Name	Conn.
43	GND	GND
44	TX4+	PCIe
45	TX4-	PCIe
46	GND	GND
47	RX4+	PCIe
48	RX4-	PCIe
49	GND	GND
50	TX5+	-
51	TX5-	-
52	GND	GND
53	RX5+	-
54	RX5-	-
55	GND	GND
56	SCL_L	MMC
57	PWR	+12V
58	GND	GND
59	TX6+	-
60	TX6-	-
61	GND	GND
62	RX6+	-
63	RX6-	-
64	GND	GND
65	TX7+	-
66	TX7-	-
67	GND	GND
68	RX7+	-
69	RX7-	-
70	GND	GND
71	SDA_L	MMC
72	PWR	+12V
73	GND	GND
74	CLK1+	TCLKB
75	CLK1-	TCLKB
76	GND	GND
77	CLK2+	TCLKA
78	CLK2-	TCLKA
79	GND	GND
80	CLK3+	PCIeCLK
81	CLK3-	PCIeCLK
82	GND	GND
83	PS0#	Diode PS1
84	PWR	+12V

No.	Name	Conn.
170	GND	CPLD (PU)
169	TDI	CPLD (PU)
168	TDO	CPLD (PU)
167	TRST#	-
166	TMS	CPLD (PU)
165	TCK	CPLD (PD)
164	GND	GND
163	TX20+	TX20
162	TX20-	TX20
161	GND	GND
160	RX20+	FPGA MLVDS
159	RX20-	FPGA MLVDS
158	GND	GND
157	TX19+	FPGA MLVDS
156	TX19-	FPGA MLVDS
155	GND	GND
154	RX19+	FPGA MLVDS
153	RX19-	FPGA MLVDS
152	GND	GND
151	TX18+	FPGA MLVDS
150	TX18-	FPGA MLVDS
149	GND	GND
148	RX18+	FPGA MLVDS
147	RX18-	FPGA MLVDS
146	GND	GND
145	TX17+	FPGA MLVDS
144	TX17-	FPGA MLVDS
143	GND	GND
142	RX17+	RX17
141	RX17-	RX17
140	GND	GND
139	TX16+	FPGA MLVDS
138	TX16-	FPGA MLVDS
137	GND	GND
136	RX16+	FPGA MLVDS
135	RX16-	FPGA MLVDS
134	GND	GND
133	TX15+	FPGA MLVDS
132	TX15-	FPGA MLVDS
131	GND	GND
130	RX15+	FPGA MGT
129	RX15-	FPGA MGT

No.	Name	Conn.
128	GND	GND
127	TX14+	FPGA MGT
126	TX14-	FPGA MGT
125	GND	GND
124	RX14+	FPGA MGT
123	RX14-	FPGA MGT
122	GND	GND
121	TX13+	FPGA MGT
120	TX13-	FPGA MGT
119	GND	GND
118	RX13+	FPGA MGT
117	RX13-	FPGA MGT
116	GND	GND
115	TX12+	FPGA MGT
114	TX12-	FPGA MGT
113	GND	GND
112	RX12+	FPGA MGT
111	RX12-	FPGA MGT
110	GND	GND
109	TX11+	-
108	TX11-	-
107	GND	GND
105	RX11-	-
104	GND	GND
103	TX10+	-
102	TX10-	-
101	GND	GND
100	RX10+	-
99	RX10-	-
98	GND	GND
97	TX9+	-
96	TX9-	-
95	GND	GND
94	RX9+	-
93	RX9-	-
92	GND	GND
91	TX8+	-
90	TX8-	-
89	GND	GND
88	RX8+	-
87	RX8-	-
86	GND	GND

2.10.6 FMC Low Pin Count (LPC) connector

Presented in the below table:

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	n.c.	GND	NC	NC	3V3 power good	GND	NC	NC
2	NC	NC	FMC1_PRSNT	FMC1_CLK0_C2M_P	NC	NC	GND	FMC1_DP0_C2M_P	NC	NC
3	NC	NC	GND	FMC1_CLK0_C2M_N	NC	NC	GND	FMC1_DP0_C2M_N	NC	NC
4	NC	NC	FMC1_CLK0_M2C_P	GND	NC	NC	FMC1_GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	FMC1_CLK0_M2C_N	GND	NC	NC	FMC1_GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	FMC1_LA00_CC_P	NC	NC	GND	FMC1_DP0_M2C_P	NC	NC
7	NC	NC	FMC1_LA02_P	FMC1_LA00_CC_N	NC	NC	GND	FMC1_DP0_M2C_N	NC	NC
8	NC	NC	FMC1_LA02_N	GND	NC	NC	FMC1_LA01_CC_P	GND	NC	NC
9	NC	NC	GND	FMC1_LA03_P	NC	NC	FMC1_LA01_CC_N	GND	NC	NC
10	NC	NC	FMC1_LA04_P	FMC1_LA03_N	NC	NC	GND	FMC1_LA06_P	NC	NC
11	NC	NC	FMC1_LA04_N	GND	NC	NC	FMC1_LA05_P	FMC1_LA06_N	NC	NC
12	NC	NC	GND	FMC1_LA08_P	NC	NC	FMC1_LA05_N	GND	NC	NC
13	NC	NC	FMC1_LA07_P	FMC1_LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	FMC1_LA07_N	GND	NC	NC	FMC1_LA09_P	FMC1_LA10_P	NC	NC
15	NC	NC	GND	FMC1_LA12_P	NC	NC	FMC1_LA09_N	FMC1_LA10_N	NC	NC
16	NC	NC	FMC1_LA11_P	FMC1_LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	FMC1_LA11_N	GND	NC	NC	FMC1_LA13_P	GND	NC	NC
18	NC	NC	GND	FMC1_LA16_P	NC	NC	FMC1_LA13_N	FMC1_LA14_P	NC	NC
19	NC	NC	FMC1_LA15_P	FMC1_LA16_N	NC	NC	GND	FMC1_LA14_N	NC	NC
20	NC	NC	FMC1_LA15_N	GND	NC	NC	FMC1_LA17_CC_P	GND	NC	NC
21	NC	NC	GND	FMC1_LA20_P	NC	NC	FMC1_LA17_CC_N	GND	NC	NC
22	NC	NC	FMC1_LA19_P	FMC1_LA20_N	NC	NC	GND	FMC1_LA18_CC_P	NC	NC
23	NC	NC	FMC1_LA19_N	GND	NC	NC	FMC1_LA23_P	FMC1_LA18_CC_N	NC	NC
24	NC	NC	GND	FMC1_LA22_P	NC	NC	FMC1_LA23_N	GND	NC	NC
25	NC	NC	FMC1_LA21_P	FMC1_LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	FMC1_LA21_N	GND	NC	NC	FMC1_LA26_P	FMC1_LA27_P	NC	NC
27	NC	NC	GND	FMC1_LA25_P	NC	NC	FMC1_LA26_N	FMC1_LA27_N	NC	NC
28	NC	NC	FMC1_LA24_P	FMC1_LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	FMC1_LA24_N	GND	NC	NC	FMC1_TCK	GND	NC	NC
30	NC	NC	GND	FMC1_LA29_P	NC	NC	FMC1_TDI	FMC1_SCL	NC	NC
31	NC	NC	FMC1_LA28_P	FMC1_LA29_N	NC	NC	FMC1_TDO	FMC1_SDA	NC	NC
32	NC	NC	FMC1_LA28_N	GND	NC	NC	3V3	GND	NC	NC
33	NC	NC	GND	FMC1_LA31_P	NC	NC	FMC1_TMS	GND	NC	NC
34	NC	NC	FMC1_LA30_P	FMC1_LA31_N	NC	NC	3V3 P	GND (GA0)	NC	NC
35	NC	NC	FMC1_LA30_N	GND	NC	NC	GND (GA1)	12V	NC	NC
36	NC	NC	GND	FMC1_LA33_P	NC	NC	3V3	GND	NC	NC
37	NC	NC	FMC1_LA32_P	FMC1_LA33_N	NC	NC	GND	12V	NC	NC
38	NC	NC	FMC1_LA32_N	GND	NC	NC	3V3	GND	NC	NC
39	NC	NC	GND	2V5, fixed	NC	NC	GND	3V3	NC	NC
40	NC	NC	2V5, fixed	GND	NC	NC	3V3	GND	NC	NC

2.10.7 FMC High Pin Count (HPC) Connector

Presented in the below tables:

	K	J	H	G	F
1	NC	GND	NC	GND	PD
2	GND	FMC2_CLK3_BIDIR_P	FMC2_PRSNT	FMC2_CLK0_C2M_P	GND
3	GND	FMC2_CLK3_BIDIR_N	GND	FMC2_CLK0_C2M_N	GND
4	FMC2_CLK2_BIDIR_P	GND	FMC2_CLK0_M2C_P	GND	FMC2_HA00_CC_P
5	FMC2_CLK2_BIDIR_N	GND	FMC2_CLK0_M2C_N	GND	FMC2_HA00_CC_N
6	GND	FMC2_HA03_P	GND	FMC2_LA00_CC_P	GND
7	FMC2_HA02_P	FMC2_HA03_N	FMC2_LA02_P	FMC2_LA00_CC_N	FMC2_HA04_P
8	FMC2_HA02_N	GND	FMC2_LA02_N	GND	FMC2_HA04_N
9	GND	FMC2_HA07_P	GND	FMC2_LA03_P	GND
10	FMC2_HA06_P	FMC2_HA07_N	FMC2_LA04_P	FMC2_LA03_N	FMC2_HA08_P
11	FMC2_HA06_N	GND	FMC2_LA04_N	GND	FMC2_HA08_N
12	GND	FMC2_HA11_P	GND	FMC2_LA08_P	GND
13	FMC2_HA10_P	FMC2_HA11_N	FMC2_LA07_P	FMC2_LA08_N	FMC2_HA12_P
14	FMC2_HA10_N	GND	FMC2_LA07_N	GND	FMC2_HA12_N
15	GND	FMC2_HA14_P	GND	FMC2_LA12_P	GND
16	FMC2_HA17_CC_P	FMC2_HA14_N	FMC2_LA11_P	FMC2_LA12_N	FMC2_HA15_P
17	FMC2_HA17_CC_N	GND	FMC2_LA11_N	GND	FMC2_HA15_N
18	GND	FMC2_HA18_P	GND	FMC2_LA16_P	GND
19	FMC2_HA21_P	FMC2_HA18_N	FMC2_LA15_P	FMC2_LA16_N	FMC2_HA19_P
20	FMC2_HA21_N	GND	FMC2_LA15_N	GND	FMC2_HA19_N
21	GND	FMC2_HA22_P	GND	FMC2_LA20_P	GND
22	FMC2_HA23_P	FMC2_HA22_N	FMC2_LA19_P	FMC2_LA20_N	FMC2_HB02_P
23	FMC2_HA23_N	GND	FMC2_LA19_N	GND	FMC2_HB02_N
24	GND	FMC2_HB01_P	GND	FMC2_LA22_P	GND
25	FMC2_HB00_CC_P	FMC2_HB01_N	FMC2_LA21_P	FMC2_LA22_N	FMC2_HB04_P
26	FMC2_HB00_CC_N	GND	FMC2_LA21_N	GND	FMC2_HB04_N
27	GND	FMC2_HB07_P	GND	FMC2_LA25_P	GND
28	FMC2_HB06_CC_P	FMC2_HB07_N	FMC2_LA24_P	FMC2_LA25_N	FMC2_HB08_P
29	FMC2_HB06_CC_N	GND	FMC2_LA24_N	GND	FMC2_HB08_N
30	GND	FMC2_HB11_P	GND	FMC2_LA29_P	GND
31	FMC2_HB10_P	FMC2_HB11_N	FMC2_LA28_P	FMC2_LA29_N	FMC2_HB12_P
32	FMC2_HB10_N	GND	FMC2_LA28_N	GND	FMC2_HB12_N
33	GND	FMC2_HB15_P	GND	FMC2_LA31_P	GND
34	FMC2_HB14_P	FMC2_HB15_N	FMC2_LA30_P	FMC2_LA31_N	FMC2_HB16_P
35	FMC2_HB14_N	GND	FMC2_LA30_N	GND	FMC2_HB16_N
36	GND	FMC2_HB18_P	GND	FMC2_LA33_P	GND
37	FMC2_HB17_CC_P	FMC2_HB18_N	FMC2_LA32_P	FMC2_LA33_N	FMC2_HB20_P
38	FMC2_HB17_CC_N	GND	FMC2_LA32_N	GND	FMC2_HB20_N
39	GND	FMC2_VIOB (VCCO4)	GND	2V5, fixed	GND
40	FMC2_VIOB (VCCO4)	GND	2V5, fixed	GND	2V5, fixed

	E	D	C	B	A
1	GND	3V3 power good	GND	NC	GND
2	FMC2_HA01_CC_P	GND	FMC2_DP0_C2M_P	GND	NC
3	FMC2_HA01_CC_N	GND	FMC2_DP0_C2M_N	GND	NC
4	GND	FMC2_GBTCLK0_M2C_P	GND	NC	GND
5	GND	FMC2_GBTCLK0_M2C_N	GND	NC	GND
6	FMC2_HA05_CC_P	GND	FMC2_DP0_M2C_P	GND	NC
7	FMC2_HA05_CC_N	GND	FMC2_DP0_M2C_N	GND	NC
8	GND	FMC2_LA01_CC_P	GND	NC	GND
9	FMC2_HA09_P	FMC2_LA01_CC_N	GND	NC	GND
10	FMC2_HA09_N	GND	FMC2_LA06_P	GND	NC
11	GND	FMC2_LA05_P	FMC2_LA06_N	GND	NC
12	FMC2_HA13_P	FMC2_LA05_N	GND	NC	GND
13	FMC2_HA13_N	GND	GND	NC	GND
14	GND	FMC2_LA09_P	FMC2_LA10_P	GND	NC
15	FMC2_HA16_P	FMC2_LA09_N	FMC2_LA10_N	GND	NC
16	FMC2_HA16_N	GND	GND	NC	GND
17	GND	FMC2_LA13_P	GND	NC	GND
18	FMC2_HA20_P	FMC2_LA13_N	FMC2_LA14_P	GND	NC
19	FMC2_HA20_N	GND	FMC2_LA14_N	GND	NC
20	GND	FMC2_LA17_CC_P	GND	NC	GND
21	FMC2_HB03_P	FMC2_LA17_CC_N	GND	NC	GND
22	FMC2_HB03_N	GND	FMC2_LA18_CC_P	GND	NC
23	GND	FMC2_LA23_P	FMC2_LA18_CC_N	GND	NC
24	FMC2_HB05_P	FMC2_LA23_N	GND	NC	GND
25	FMC2_HB05_N	GND	GND	NC	GND
26	GND	FMC2_LA26_P	FMC2_LA27_P	GND	NC
27	FMC2_HB09_P	FMC2_LA26_N	FMC2_LA27_N	GND	NC
28	FMC2_HB09_N	GND	GND	NC	GND
29	GND	FMC2_TCK	GND	NC	GND
30	FMC2_HB13_P	FMC2_TDI	FMC2_SCL	GND	NC
31	FMC2_HB13_N	FMC2_TDO	FMC2_SDA	GND	NC
32	GND	3V3	GND	NC	GND
33	FMC2_HB19_P	FMC2_TMS	GND	NC	GND
34	FMC2_HB19_N	3V3 PU	3V3 (GA0)	GND	NC
35	GND	GND (GA1)	12V	GND	NC
36	FMC2_HB21_P	3V3	GND	NC	GND
37	FMC2_HB21_N	GND	12V	NC	GND
38	GND	3V3	GND	GND	NC
39	2V5	GND	3V3	GND	NC
40	GND	3V3	GND	NC	GND

2.11 Pinout for FPGAs

2.11.1 UCF for Main FPGA

```
##############################################
##          UCF FOR DAMC-FMC20 XC6SLX150
##############################################

                    #FPGA SPI
#NET     "FPGA_CS"              LOC =  "A26";
#NET     "FPGA_INIT"            LOC =  "AJ6";
#NET     "FPGA_MISO"            LOC =  "A27";
#NET     "FPGA_MOSI"            LOC =  "D26";
#NET     "FPGA_SCK"             LOC =  "B27";

                    #Clocks
#NET     "PCIECLK2_N"           LOC =  "W4";
#NET     "PCIECLK2_P"           LOC =  "W5";
#NET     "TCLKA0_N"             LOC =  "W30";
#NET     "TCLKA0_P"             LOC =  "W29";
#NET     "TCLKB0_N"             LOC =  "V27";
#NET     "TCLKB0_P"             LOC =  "V26";
#NET     "12MHZ"                LOC =  "K26";

                    #Chip-to-Chip-Bus
#NET     "INTER_ALE_N"          LOC =  "B30";
#NET     "INTER_ALE_P"          LOC =  "B29";
#NET     "INTER_B_CLK_N"        LOC =  "C30";
#NET     "INTER_B_CLK_P"        LOC =  "C29";
#NET     "INTER_B0"             LOC =  "N28";
#NET     "INTER_B1"             LOC =  "R27";
#NET     "INTER_B10"            LOC =  "Y27";
#NET     "INTER_B11"            LOC =  "AA28";
#NET     "INTER_B12"            LOC =  "K28";
#NET     "INTER_B13"            LOC =  "Y30";
#NET     "INTER_B14"            LOC =  "P25";
#NET     "INTER_B15"            LOC =  "Y24";
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#NET    "INTER_B16"          LOC =  "T27";
#NET    "INTER_B17"          LOC =  "R25";
#NET    "INTER_B18"          LOC =  "AD30";
#NET    "INTER_B19"          LOC =  "U28";
#NET    "INTER_B2"           LOC =  "AA29";
#NET    "INTER_B20"          LOC =  "E27";
#NET    "INTER_B21"          LOC =  "T26";
#NET    "INTER_B22"          LOC =  "V28";
#NET    "INTER_B23"          LOC =  "AC30";
#NET    "INTER_B24"          LOC =  "U29";
#NET    "INTER_B25"          LOC =  "V30";
#NET    "INTER_B26"          LOC =  "U27";
#NET    "INTER_B27"          LOC =  "U30";
#NET    "INTER_B28"          LOC =  "R28";
#NET    "INTER_B29"          LOC =  "T28";
#NET    "INTER_B3"           LOC =  "F26";
#NET    "INTER_B30"          LOC =  "D27";
#NET    "INTER_B31"          LOC =  "P27";
#NET    "INTER_B32"          LOC =  "T30";
#NET    "INTER_B33"          LOC =  "R29";
#NET    "INTER_B34"          LOC =  "P30";
#NET    "INTER_B35"          LOC =  "M30";
#NET    "INTER_B36"          LOC =  "R30";
#NET    "INTER_B37"          LOC =  "P28";
#NET    "INTER_B38"          LOC =  "K30";
#NET    "INTER_B39"          LOC =  "J30";
#NET    "INTER_B4"           LOC =  "N29";
#NET    "INTER_B40"          LOC =  "J29";
#NET    "INTER_B41"          LOC =  "G28";
#NET    "INTER_B42"          LOC =  "L29";
#NET    "INTER_B43"          LOC =  "L27";
#NET    "INTER_B44"          LOC =  "M28";
#NET    "INTER_B45"          LOC =  "M27";
#NET    "INTER_B46"          LOC =  "J28";
#NET    "INTER_B47"          LOC =  "L30";
#NET    "INTER_B48"          LOC =  "E28";
#NET    "INTER_B49"          LOC =  "W24";
```

```
#NET    "INTER_B5"          LOC =  "M26";
#NET    "INTER_B50"         LOC =  "AA27";
#NET    "INTER_B51"         LOC =  "Y25";
#NET    "INTER_B52"         LOC =  "L28";
#NET    "INTER_B53"         LOC =  "Y26";
#NET    "INTER_B54"         LOC =  "H26";
#NET    "INTER_B55"         LOC =  "J27";
#NET    "INTER_B56"         LOC =  "D28";
#NET    "INTER_B57"         LOC =  "H27";
#NET    "INTER_B58"         LOC =  "H30";
#NET    "INTER_B59"         LOC =  "G29";
#NET    "INTER_B6"          LOC =  "Y28";
#NET    "INTER_B60"         LOC =  "G27";
#NET    "INTER_B61"         LOC =  "F27";
#NET    "INTER_B62"         LOC =  "F30";
#NET    "INTER_B63"         LOC =  "G30";
#NET    "INTER_B7"          LOC =  "AA30";
#NET    "INTER_B8"          LOC =  "P26";
#NET    "INTER_B9"          LOC =  "C27";
#NET    "INTER_RE_N"        LOC =  "A29";
#NET    "INTER_RE_P"        LOC =  "A28";
#NET    "INTER_WE_N"        LOC =  "E30";
#NET    "INTER_WE_P"        LOC =  "E29";
```

#Clock Loop

```
#NET    "CLK_AUX1"          LOC =  "U7";
#NET    "CLK_AUX1"          LOC =  "V4";
#NET    "CLK_AUX2"          LOC =  "U6";
#NET    "CLK_AUX2"          LOC =  "V3";
```

#Debug

```
#NET    "S150_LED1"         LOC =  "AH1";
#NET    "S150_LED2"         LOC =  "AJ1";
#NET    "S150_LED3"         LOC =  "AK2";
#NET    "S150_RX"           LOC =  "E26";
#NET    "S150_TX"           LOC =  "D30";
```

```
                    # Platform FLASH
#NET     "XCF16_CCLK"           LOC =  "AJ26";
#NET     "XCF16_M1"             LOC =  "AJ22";
#NET     "XCF16_CSI_B"          LOC =  "AK25";
#NET     "XCF16_D0"             LOC =  "AH25";
#NET     "XCF16_RDWD_B"         LOC =  "AK11";
#NET     "XCF16_M0"             LOC =  "AK26";

                    #RTM J31
#NET     "RTM_D24_N"            LOC =  "AE16";
#NET     "RTM_D24_P"            LOC =  "AD16";
#NET     "RTM_D25_N"            LOC =  "AH10";
#NET     "RTM_D25_P"            LOC =  "AG10";
#NET     "RTM_D26_N"            LOC =  "AE14";
#NET     "RTM_D26_P"            LOC =  "AD14";
#NET     "RTM_D27_N"            LOC =  "AE13";
#NET     "RTM_D27_P"            LOC =  "AD13";
#NET     "RTM_D28_N"            LOC =  "AK14";
#NET     "RTM_D28_P"            LOC =  "AJ14";
#NET     "RTM_D29_N"            LOC =  "AK13";
#NET     "RTM_D29_P"            LOC =  "AH13";
#NET     "RTM_D30_N"            LOC =  "AK12";
#NET     "RTM_D30_P"            LOC =  "AJ12";
#NET     "RTM_D31_N"            LOC =  "AK10";
#NET     "RTM_D31_P"            LOC =  "AJ10";
#NET     "RTM_D32_N"            LOC =  "AE10";
#NET     "RTM_D32_P"            LOC =  "AD10";
 #NET    "RTM_D33_N"            LOC =  "AE9";
 #NET    "RTM_D33_P"            LOC =  "AD9";
#NET     "RTM_D34_N"            LOC =  "AH14";
#NET     "RTM_D34_P"            LOC =  "AG14";
#NET     "RTM_D35_N"            LOC =  "AB15";
#NET     "RTM_D35_P"            LOC =  "AA15";
#NET     "RTM_D36_N"            LOC =  "AC14";
#NET     "RTM_D36_P"            LOC =  "AB14";
#NET     "RTM_D37_N"            LOC =  "AG13";
#NET     "RTM_D37_P"            LOC =  "AF13";
```

```
#NET    "RTM_D38_N"          LOC =  "AH12";
#NET    "RTM_D38_P"          LOC =  "AG12";
#NET    "RTM_D39_N"          LOC =  "AC12";
#NET    "RTM_D39_P"          LOC =  "AB12";
#NET    "RTM_D40_N"          LOC =  "AG11";
#NET    "RTM_D40_P"          LOC =  "AF11";
#NET    "RTM_D41_N"          LOC =  "AK9";
#NET    "RTM_D41_P"          LOC =  "AH9";
#NET    "RTM_D42_N"          LOC =  "AK8";
#NET    "RTM_D42_P"          LOC =  "AJ8";
#NET    "RTM_D43_N"          LOC =  "AE8";
#NET    "RTM_D43_P"          LOC =  "AD8";
#NET    "RTM_D44_N"          LOC =  "AC16";
#NET    "RTM_D44_P"          LOC =  "AB16";
#NET    "RTM_D45_N"          LOC =  "AE15";
#NET    "RTM_D45_P"          LOC =  "AD15";
#NET    "RTM_D46_N"          LOC =  "AG9";
#NET    "RTM_D46_P"          LOC =  "AF9";
#NET    "RTM_D47_N"          LOC =  "AK15";
#NET    "RTM_D47_P"          LOC =  "AH15";
#NET    "RTM_D48_N"          LOC =  "AH8";
#NET    "RTM_D48_P"          LOC =  "AG8";
#NET    "RTM_D49_N"          LOC =  "AE12";
#NET    "RTM_D49_P"          LOC =  "AD12";
#NET    "RTM_D50_N"          LOC =  "AD11";
#NET    "RTM_D50_P"          LOC =  "AB11";
#NET    "RTM_D51_N"          LOC =  "AG7";
#NET    "RTM_D51_P"          LOC =  "AF7";
#NET    "RTM_D52_N"          LOC =  "AH6";
#NET    "RTM_D52_P"          LOC =  "AG6";
#NET    "RTM_D53_N"          LOC =  "AK7";
#NET    "RTM_D53_P"          LOC =  "AH7";
```

 # RTM J30

```
#NET    "AMC_CLK_N"          LOC =  "W28";
#NET    "AMC_CLK_P"          LOC =  "W27";
#NET    "RTM_CLK_N"          LOC =  "AB30";
```

```
#NET    "RTM_CLK_P"          LOC =  "AB28";
#NET    "RTM_D10_N"          LOC =  "AK23";
#NET    "RTM_D10_P"          LOC =  "AH23";
#NET    "RTM_D11_N"          LOC =  "AH20";
#NET    "RTM_D11_P"          LOC =  "AG20";
#NET    "RTM_D12_N"          LOC =  "AC18";
#NET    "RTM_D12_P"          LOC =  "AB18";
#NET    "RTM_D13_N"          LOC =  "AE19";
#NET    "RTM_D13_P"          LOC =  "AD19";
#NET    "RTM_D14_N"          LOC =  "AH16";
#NET    "RTM_D14_P"          LOC =  "AG16";
#NET    "RTM_D15_N"          LOC =  "AG17";
#NET    "RTM_D15_P"          LOC =  "AF17";
#NET    "RTM_D16_N"          LOC =  "AH22";
#NET    "RTM_D16_P"          LOC =  "AG22";
#NET    "RTM_D17_N"          LOC =  "AG23";
#NET    "RTM_D17_P"          LOC =  "AF23";
#NET    "RTM_D18_N"          LOC =  "AG21";
#NET    "RTM_D18_P"          LOC =  "AF21";
#NET    "RTM_D19_N"          LOC =  "AB19";
#NET    "RTM_D19_P"          LOC =  "AA19";
#NET    "RTM_D2_N"           LOC =  "AE22";
#NET    "RTM_D2_P"           LOC =  "AD22";
#NET    "RTM_D20_N"          LOC =  "AE20";
#NET    "RTM_D20_P"          LOC =  "AD20";
#NET    "RTM_D21_N"          LOC =  "AE17";
#NET    "RTM_D21_P"          LOC =  "AD17";
#NET    "RTM_D22_N"          LOC =  "AE18";
#NET    "RTM_D22_P"          LOC =  "AD18";
#NET    "RTM_D23_N"          LOC =  "AG15";
#NET    "RTM_D23_P"          LOC =  "AF15";
#NET    "RTM_D3_N"           LOC =  "AD21";
#NET    "RTM_D3_P"           LOC =  "AC21";
#NET    "RTM_D4_N"           LOC =  "AG19";
#NET    "RTM_D4_P"           LOC =  "AF19";
#NET    "RTM_D5_N"           LOC =  "AH18";
#NET    "RTM_D5_P"           LOC =  "AG18";
```

```
#NET    "RTM_D6_N"          LOC =  "AK21";
#NET    "RTM_D6_P"          LOC =  "AH21";
#NET    "RTM_D7_N"          LOC =  "AK20";
#NET    "RTM_D7_P"          LOC =  "AJ20";
#NET    "RTM_D9_N"          LOC =  "AC20";
#NET    "RTM_D9_P"          LOC =  "AB20";
#NET    "RTM_D1_N"          LOC =  "AE23";
#NET    "RTM_D1_P"          LOC =  "AD23";
```

#AMC MLVDS Signals

```
#NET    "AMC_RX17_DE"       LOC =  "AE28";
#NET    "AMC_RX17_DI"       LOC =  "AD28";
#NET    "AMC_RX17_DO"       LOC =  "AH30";
#NET    "AMC_RX18_DE"       LOC =  "AE29";
#NET    "AMC_RX18_DI"       LOC =  "AF30";
#NET    "AMC_RX18_DO"       LOC =  "AJ29";
#NET    "AMC_RX19_DE"       LOC =  "AF28";
#NET    "AMC_RX19_DI"       LOC =  "AG29";
#NET    "AMC_RX19_DO"       LOC =  "AK27";
#NET    "AMC_RX20_DE"       LOC =  "AC27";
#NET    "AMC_RX20_DI"       LOC =  "AG27";
#NET    "AMC_RX20_DO"       LOC =  "AK28";
#NET    "AMC_TX17_DE"       LOC =  "AE30";
#NET    "AMC_TX17_DI"       LOC =  "AC28";
#NET    "AMC_TX17_DO"       LOC =  "AJ30";
#NET    "AMC_TX18_DE"       LOC =  "AD27";
#NET    "AMC_TX18_DI"       LOC =  "AG30";
#NET    "AMC_TX18_DO"       LOC =  "AK29";
#NET    "AMC_TX19_DE"       LOC =  "AC29";
#NET    "AMC_TX19_DI"       LOC =  "AG28";
#NET    "AMC_TX19_DO"       LOC =  "AH27";
#NET    "AMC_TX20_DE"       LOC =  "AE27";
#NET    "AMC_TX20_DI"       LOC =  "AD26";
#NET    "AMC_TX20_DO"       LOC =  "AJ28";
```

 # FMC LPC

```
#NET    "FMC1_CLK0_C2M_N"   LOC =  "AK19";
```

```
#NET    "FMC1_CLK0_C2M_P"     LOC =  "AH19";
#NET    "FMC1_CLK0_M2C_N"     LOC =  "AK18";
#NET    "FMC1_CLK0_M2C_P"     LOC =  "AJ18";
 #NET    "FMC1_LA00_CC_N"      LOC =  "A18";
 #NET    "FMC1_LA00_CC_P"      LOC =  "C18";
 #NET    "FMC1_LA01_CC_N"      LOC =  "A16";
 #NET    "FMC1_LA01_CC_P"      LOC =  "C16";
#NET    "FMC1_LA02_N"         LOC =  "AG25";
#NET    "FMC1_LA02_P"         LOC =  "AF25";
#NET    "FMC1_LA03_N"         LOC =  "AH24";
#NET    "FMC1_LA03_P"         LOC =  "AG24";
 #NET    "FMC1_LA04_N"         LOC =  "C25";
 #NET    "FMC1_LA04_P"         LOC =  "D25";
 #NET    "FMC1_LA05_N"         LOC =  "F23";
 #NET    "FMC1_LA05_P"         LOC =  "G23";
 #NET    "FMC1_LA06_N"         LOC =  "A24";
 #NET    "FMC1_LA06_P"         LOC =  "C24";
 #NET    "FMC1_LA07_N"         LOC =  "F22";
 #NET    "FMC1_LA07_P"         LOC =  "G22";
 #NET    "FMC1_LA08_N"         LOC =  "H21";
 #NET    "FMC1_LA08_P"         LOC =  "J21";
 #NET    "FMC1_LA09_N"         LOC =  "D24";
 #NET    "FMC1_LA09_P"         LOC =  "E24";
 #NET    "FMC1_LA10_N"         LOC =  "A23";
 #NET    "FMC1_LA10_P"         LOC =  "B23";
 #NET    "FMC1_LA11_N"         LOC =  "C23";
 #NET    "FMC1_LA11_P"         LOC =  "D23";
 #NET    "FMC1_LA12_N"         LOC =  "F21";
 #NET    "FMC1_LA12_P"         LOC =  "G21";
 #NET    "FMC1_LA13_N"         LOC =  "C21";
 #NET    "FMC1_LA13_P"         LOC =  "D21";
 #NET    "FMC1_LA14_N"         LOC =  "A22";
 #NET    "FMC1_LA14_P"         LOC =  "C22";
 #NET    "FMC1_LA15_N"         LOC =  "D22";
 #NET    "FMC1_LA15_P"         LOC =  "E22";
 #NET    "FMC1_LA16_N"         LOC =  "G20";
 #NET    "FMC1_LA16_P"         LOC =  "J20";
```


```
#NET    "FMC1_LA17_CC_N"      LOC =  "A21";
#NET    "FMC1_LA17_CC_P"      LOC =  "B21";
#NET    "FMC1_LA18_CC_N"      LOC =  "A20";
#NET    "FMC1_LA18_CC_P"      LOC =  "C20";
#NET    "FMC1_LA19_N"         LOC =  "H19";
#NET    "FMC1_LA19_P"         LOC =  "J19";
#NET    "FMC1_LA20_N"         LOC =  "D20";
#NET    "FMC1_LA20_P"         LOC =  "E20";
#NET    "FMC1_LA21_N"         LOC =  "F19";
#NET    "FMC1_LA21_P"         LOC =  "G19";
#NET    "FMC1_LA22_N"         LOC =  "C19";
#NET    "FMC1_LA22_P"         LOC =  "D19";
#NET    "FMC1_LA23_N"         LOC =  "A19";
#NET    "FMC1_LA23_P"         LOC =  "B19";
#NET    "FMC1_LA24_N"         LOC =  "H17";
#NET    "FMC1_LA24_P"         LOC =  "J17";
#NET    "FMC1_LA25_N"         LOC =  "D18";
#NET    "FMC1_LA25_P"         LOC =  "E18";
#NET    "FMC1_LA26_N"         LOC =  "F18";
#NET    "FMC1_LA26_P"         LOC =  "G18";
#NET    "FMC1_LA27_N"         LOC =  "A25";
#NET    "FMC1_LA27_P"         LOC =  "B25";
#NET    "FMC1_LA28_N"         LOC =  "F17";
#NET    "FMC1_LA28_P"         LOC =  "G17";
#NET    "FMC1_LA29_N"         LOC =  "C17";
#NET    "FMC1_LA29_P"         LOC =  "D17";
#NET    "FMC1_LA30_N"         LOC =  "F16";
#NET    "FMC1_LA30_P"         LOC =  "G16";
#NET    "FMC1_LA31_N"         LOC =  "D16";
#NET    "FMC1_LA31_P"         LOC =  "E16";
#NET    "FMC1_LA32_N"         LOC =  "A17";
#NET    "FMC1_LA32_P"         LOC =  "B17";
#NET    "FMC1_LA33_N"         LOC =  "F15";
#NET    "FMC1_LA33_P"         LOC =  "G15";
```

 # FMC HPC

```
#NET    "FMC2_CLK2_BIDIR_N"   LOC =  "AA1";
```

```
#NET    "FMC2_CLK2_BIDIR_P"   LOC =  "AA3";
#NET    "FMC2_CLK3_BIDIR_N"   LOC =  "AB1";
#NET    "FMC2_CLK3_BIDIR_P"   LOC =  "AB2";
#NET    "FMC2_HA00_CC_N"      LOC =  "AB3";
#NET    "FMC2_HA00_CC_P"      LOC =  "AB4";
#NET    "FMC2_HA01_CC_N"      LOC =  "AD3";
#NET    "FMC2_HA01_CC_P"      LOC =  "AD4";
#NET    "FMC2_HA02_N"         LOC =  "V7";
#NET    "FMC2_HA02_P"         LOC =  "V8";
#NET    "FMC2_HA03_N"         LOC =  "Y3";
#NET    "FMC2_HA03_P"         LOC =  "Y4";
#NET    "FMC2_HA04_N"         LOC =  "U4";
#NET    "FMC2_HA04_P"         LOC =  "U5";
#NET    "FMC2_HA05_N"         LOC =  "W6";
#NET    "FMC2_HA05_P"         LOC =  "W7";
#NET    "FMC2_HA06_N"         LOC =  "R4";
#NET    "FMC2_HA06_P"         LOC =  "R5";
#NET    "FMC2_HA07_N"         LOC =  "T3";
#NET    "FMC2_HA07_P"         LOC =  "T4";
#NET    "FMC2_HA08_N"         LOC =  "M6";
#NET    "FMC2_HA08_P"         LOC =  "M7";
#NET    "FMC2_HA09_N"         LOC =  "P6";
#NET    "FMC2_HA09_P"         LOC =  "P7";
#NET    "FMC2_HA10_N"         LOC =  "R1";
#NET    "FMC2_HA10_P"         LOC =  "R3";
#NET    "FMC2_HA11_N"         LOC =  "N4";
#NET    "FMC2_HA11_P"         LOC =  "N5";
#NET    "FMC2_HA12_N"         LOC =  "T1";
#NET    "FMC2_HA12_P"         LOC =  "T2";
#NET    "FMC2_HA13_N"         LOC =  "P3";
#NET    "FMC2_HA13_P"         LOC =  "P4";
#NET    "FMC2_HA14_N"         LOC =  "U1";
#NET    "FMC2_HA14_P"         LOC =  "U3";
#NET    "FMC2_HA15_N"         LOC =  "W1";
#NET    "FMC2_HA15_P"         LOC =  "W3";
#NET    "FMC2_HA16_N"         LOC =  "V1";
#NET    "FMC2_HA16_P"         LOC =  "V2";
```

```
#NET    "FMC2_HA17_CC_N"      LOC =  "Y1";
#NET    "FMC2_HA17_CC_P"      LOC =  "Y2";
#NET    "FMC2_HA18_N"         LOC =  "AC1";
#NET    "FMC2_HA18_P"         LOC =  "AC3";
#NET    "FMC2_HA19_N"         LOC =  "AC4";
#NET    "FMC2_HA19_P"         LOC =  "AC5";
#NET    "FMC2_HA20_N"         LOC =  "AA4";
#NET    "FMC2_HA20_P"         LOC =  "AA5";
#NET    "FMC2_HA21_N"         LOC =  "AD1";
#NET    "FMC2_HA21_P"         LOC =  "AD2";
#NET    "FMC2_HA22_N"         LOC =  "AG1";
#NET    "FMC2_HA22_P"         LOC =  "AF1";
#NET    "FMC2_HA23_N"         LOC =  "N1";
#NET    "FMC2_HA23_P"         LOC =  "N3";
#NET    "FMC2_HB00_CC_N"      LOC =  "K1";
#NET    "FMC2_HB00_CC_P"      LOC =  "K2";
#NET    "FMC2_HB01_N"         LOC =  "L1";
#NET    "FMC2_HB01_P"         LOC =  "L3";
#NET    "FMC2_HB02_N"         LOC =  "M3";
#NET    "FMC2_HB02_P"         LOC =  "M4";
#NET    "FMC2_HB03_N"         LOC =  "L6";
#NET    "FMC2_HB03_P"         LOC =  "L7";
#NET    "FMC2_HB04_N"         LOC =  "J4";
#NET    "FMC2_HB04_P"         LOC =  "J5";
#NET    "FMC2_HB05_N"         LOC =  "L4";
#NET    "FMC2_HB05_P"         LOC =  "L5";
#NET    "FMC2_HB06_CC_N"      LOC =  "H1";
#NET    "FMC2_HB06_CC_P"      LOC =  "H2";
#NET    "FMC2_HB07_N"         LOC =  "J1";
#NET    "FMC2_HB07_P"         LOC =  "J3";
#NET    "FMC2_HB08_N"         LOC =  "E4";
#NET    "FMC2_HB08_P"         LOC =  "E5";
#NET    "FMC2_HB09_N"         LOC =  "K3";
#NET    "FMC2_HB09_P"         LOC =  "K4";
#NET    "FMC2_HB10_N"         LOC =  "F1";
#NET    "FMC2_HB10_P"         LOC =  "F2";
#NET    "FMC2_HB11_N"         LOC =  "G1";
```

```
#NET    "FMC2_HB11_P"          LOC =  "G3";
#NET    "FMC2_HB12_N"          LOC =  "H3";
#NET    "FMC2_HB12_P"          LOC =  "H4";
#NET    "FMC2_HB13_N"          LOC =  "A5";
#NET    "FMC2_HB13_P"          LOC =  "B5";
#NET    "FMC2_HB14_N"          LOC =  "D1";
#NET    "FMC2_HB14_P"          LOC =  "D2";
#NET    "FMC2_HB15_N"          LOC =  "E1";
#NET    "FMC2_HB15_P"          LOC =  "E3";
#NET    "FMC2_HB16_N"          LOC =  "F3";
#NET    "FMC2_HB16_P"          LOC =  "F4";
#NET    "FMC2_HB17_CC_N"       LOC =  "A2";
#NET    "FMC2_HB17_CC_P"       LOC =  "B2";
#NET    "FMC2_HB18_N"          LOC =  "B1";
#NET    "FMC2_HB18_P"          LOC =  "C1";
#NET    "FMC2_HB19_N"          LOC =  "A4";
#NET    "FMC2_HB19_P"          LOC =  "C4";
#NET    "FMC2_HB20_N"          LOC =  "M1";
#NET    "FMC2_HB20_P"          LOC =  "M2";
#NET    "FMC2_HB21_N"          LOC =  "A3";
#NET    "FMC2_HB21_P"          LOC =  "B3";
#NET    "FMC2_CLK0_C2M_N"      LOC =  "AK16";
#NET    "FMC2_CLK0_C2M_P"      LOC =  "AJ16";
#NET    "FMC2_CLK0_M2C_N"      LOC =  "AK17";
#NET    "FMC2_CLK0_M2C_P"      LOC =  "AH17";
#NET    "FMC2_LA00_CC_N"       LOC =  "A15";
#NET    "FMC2_LA00_CC_P"       LOC =  "B15";
#NET    "FMC2_LA01_CC_N"       LOC =  "C15";
#NET    "FMC2_LA01_CC_P"       LOC =  "D15";
#NET    "FMC2_LA02_N"          LOC =  "H15";
#NET    "FMC2_LA02_P"          LOC =  "J15";
#NET    "FMC2_LA03_N"          LOC =  "A14";
#NET    "FMC2_LA03_P"          LOC =  "C14";
#NET    "FMC2_LA04_N"          LOC =  "J14";
#NET    "FMC2_LA04_P"          LOC =  "K14";
#NET    "FMC2_LA05_N"          LOC =  "F14";
#NET    "FMC2_LA05_P"          LOC =  "G14";
```

```
#NET    "FMC2_LA06_N"         LOC =  "A13";
#NET    "FMC2_LA06_P"         LOC =  "B13";
#NET    "FMC2_LA07_N"         LOC =  "F13";
#NET    "FMC2_LA07_P"         LOC =  "G13";
#NET    "FMC2_LA08_N"         LOC =  "D14";
#NET    "FMC2_LA08_P"         LOC =  "E14";
#NET    "FMC2_LA09_N"         LOC =  "H13";
#NET    "FMC2_LA09_P"         LOC =  "J13";
#NET    "FMC2_LA10_N"         LOC =  "A12";
#NET    "FMC2_LA10_P"         LOC =  "C12";
#NET    "FMC2_LA11_N"         LOC =  "D12";
#NET    "FMC2_LA11_P"         LOC =  "E12";
#NET    "FMC2_LA12_N"         LOC =  "C13";
#NET    "FMC2_LA12_P"         LOC =  "D13";
#NET    "FMC2_LA13_N"         LOC =  "A11";
#NET    "FMC2_LA13_P"         LOC =  "B11";
#NET    "FMC2_LA14_N"         LOC =  "A10";
#NET    "FMC2_LA14_P"         LOC =  "C10";
#NET    "FMC2_LA15_N"         LOC =  "C11";
#NET    "FMC2_LA15_P"         LOC =  "D11";
#NET    "FMC2_LA16_N"         LOC =  "F12";
#NET    "FMC2_LA16_P"         LOC =  "G12";
#NET    "FMC2_LA17_CC_N"      LOC =  "A9";
#NET    "FMC2_LA17_CC_P"      LOC =  "B9";
#NET    "FMC2_LA18_CC_N"      LOC =  "H11";
#NET    "FMC2_LA18_CC_P"      LOC =  "J11";
#NET    "FMC2_LA19_N"         LOC =  "J12";
#NET    "FMC2_LA19_P"         LOC =  "K12";
#NET    "FMC2_LA20_N"         LOC =  "D10";
#NET    "FMC2_LA20_P"         LOC =  "E10";
#NET    "FMC2_LA21_N"         LOC =  "F11";
#NET    "FMC2_LA21_P"         LOC =  "G11";
#NET    "FMC2_LA22_N"         LOC =  "C9";
#NET    "FMC2_LA22_P"         LOC =  "D9";
#NET    "FMC2_LA23_N"         LOC =  "A8";
#NET    "FMC2_LA23_P"         LOC =  "C8";
#NET    "FMC2_LA24_N"         LOC =  "D8";
```

```
#NET    "FMC2_LA24_P"         LOC =  "E8";
#NET    "FMC2_LA25_N"         LOC =  "A6";
#NET    "FMC2_LA25_P"         LOC =  "C6";
#NET    "FMC2_LA26_N"         LOC =  "G10";
#NET    "FMC2_LA26_P"         LOC =  "J10";
#NET    "FMC2_LA27_N"         LOC =  "A7";
#NET    "FMC2_LA27_P"         LOC =  "B7";
#NET    "FMC2_LA28_N"         LOC =  "C7";
#NET    "FMC2_LA28_P"         LOC =  "D7";
#NET    "FMC2_LA29_N"         LOC =  "F9";
#NET    "FMC2_LA29_P"         LOC =  "G9";
#NET    "FMC2_LA30_N"         LOC =  "F7";
#NET    "FMC2_LA30_P"         LOC =  "G7";
#NET    "FMC2_LA31_N"         LOC =  "F8";
#NET    "FMC2_LA31_P"         LOC =  "G8";
#NET    "FMC2_LA32_N"         LOC =  "F6";
#NET    "FMC2_LA32_P"         LOC =  "G6";
#NET    "FMC2_LA33_N"         LOC =  "D6";
  #NET    "FMC2_LA33_P"         LOC =  "E6";
```

2.11.2 UCF for Transceiver FPGA

```
##############################################
##          UCF FOR DAMC-FMC20 XC6SLX45T
##############################################

                    # AMC Clocks
NET     "TCLKA1_N"              LOC = "H3";
NET     "TCLKA1_P"              LOC = "H4";
NET     "TCLKB1_N"              LOC = "H1";
NET     "TCLKB1_P"              LOC = "H2";

                    #CONFIG
NET     "PCIE_TCK_45T"          LOC = "E14";
NET     "PCIE_TDI_45T"          LOC = "B16";
NET     "PCIE_TDO_45T"          LOC = "D15";
NET     "PCIE_TMS_45T"          LOC = "A16";
NET     "XCF8_HSWAPEN"          LOC = "B2";
NET     "XCF8_CCLK"             LOC = "R15";
NET     "XCF8_M0"               LOC = "T15";
NET     "XCF8_INT_B"            LOC = "U3";
NET     "XCF8_D0"               LOC = "R13";
NET     "XCF8_CSI_B"            LOC = "N12";
NET     "XCF8_M1"               LOC = "T13";
NET     "XCF8_RDWR_B"           LOC = "T5";

                    # Chip-Chip-Bus
NET     "INTER_RE_N"            LOC = "V5";
NET     "INTER_RE_P"            LOC = "U5";
NET     "INTER_WE_N"            LOC = "V10";
NET     "INTER_WE_P"            LOC = "U10";
NET     "INTER_ALE_N"           LOC = "V7";
NET     "INTER_ALE_P"           LOC = "U7";
NET     "INTER_B_CLK_N"         LOC = "V8";
NET     "INTER_B_CLK_P"         LOC = "U8";
NET     "INTER_B0"              LOC = "T17";
NET     "INTER_B1"              LOC = "N16";
```

```
NET    "INTER_B2"          LOC = "E16";
NET    "INTER_B3"          LOC = "P1";
NET    "INTER_B4"          LOC = "U18";
NET    "INTER_B5"          LOC = "U17";
NET    "INTER_B6"          LOC = "F17";
NET    "INTER_B7"          LOC = "F18";
NET    "INTER_B8"          LOC = "T18";
NET    "INTER_B9"          LOC = "N1";
NET    "INTER_B10"         LOC = "H15";
NET    "INTER_B11"         LOC = "H16";
NET    "INTER_B12"         LOC = "P4";
NET    "INTER_B13"         LOC = "G18";
NET    "INTER_B14"         LOC = "N17";
NET    "INTER_B15"         LOC = "K14";
NET    "INTER_B16"         LOC = "N18";
NET    "INTER_B17"         LOC = "P18";
NET    "INTER_B18"         LOC = "C18";
NET    "INTER_B19"         LOC = "K16";
NET    "INTER_B20"         LOC = "T1";
NET    "INTER_B21"         LOC = "L16";
NET    "INTER_B22"         LOC = "H17";
NET    "INTER_B23"         LOC = "C17";
NET    "INTER_B24"         LOC = "J16";
NET    "INTER_B25"         LOC = "J18";
NET    "INTER_B26"         LOC = "K17";
NET    "INTER_B27"         LOC = "K18";
NET    "INTER_B28"         LOC = "L17";
NET    "INTER_B29"         LOC = "L18";
NET    "INTER_B30"         LOC = "U1";
NET    "INTER_B31"         LOC = "M18";
NET    "INTER_B32"         LOC = "U16";
NET    "INTER_B33"         LOC = "V16";
NET    "INTER_B34"         LOC = "U13";
NET    "INTER_B35"         LOC = "V13";
NET    "INTER_B36"         LOC = "U15";
NET    "INTER_B37"         LOC = "V15";
NET    "INTER_B38"         LOC = "U11";
```

```
NET    "INTER_B39"          LOC = "V11";
NET    "INTER_B40"          LOC = "V9";
NET    "INTER_B41"          LOC = "V6";
NET    "INTER_B42"          LOC = "R11";
NET    "INTER_B43"          LOC = "T11";
NET    "INTER_B44"          LOC = "T12";
NET    "INTER_B45"          LOC = "V12";
NET    "INTER_B46"          LOC = "N10";
NET    "INTER_B47"          LOC = "P11";
NET    "INTER_B48"          LOC = "T2";
NET    "INTER_B48"          LOC = "T2";
NET    "INTER_B49"          LOC = "L14";
NET    "INTER_B50"          LOC = "E18";
NET    "INTER_B51"          LOC = "G14";
NET    "INTER_B52"          LOC = "M13";
NET    "INTER_B53"          LOC = "G16";
NET    "INTER_B54"          LOC = "N2";
NET    "INTER_B55"          LOC = "P3";
NET    "INTER_B56"          LOC = "U2";
NET    "INTER_B57"          LOC = "R7";
NET    "INTER_B58"          LOC = "T7";
NET    "INTER_B59"          LOC = "N6";
NET    "INTER_B60"          LOC = "P7";
NET    "INTER_B61"          LOC = "R3";
NET    "INTER_B62"          LOC = "T3";
NET    "INTER_B63"          LOC = "T4";
```

 # Cross-Point-Switch

```
NET    "CBS_EQ"             LOC = "D1";
NET    "CBS_I2CEN"          LOC = "L1";
NET    "CBS_PRE"            LOC = "C1";
NET    "CBS_REST"           LOC = "M1";
NET    "CBS_SCL"            LOC = "C2";
NET    "CBS_SDA"            LOC = "D2";
NET    "CBS_SWT"            LOC = "L2";
```

 # Debug

```
NET     "S45_RX"              LOC = "V4";
NET     "S45_TX"              LOC = "V3";
NET     "MP2"                 LOC = "F1";
NET     "MP3"                 LOC = "E1";
NET     "S45_LED1"            LOC = "K1";
```

3. Reference Firmware

The board is provided programmed and it can be installed into a crate and controlled using the supplied PC software tools. The following software is included:

MMC Atmel ATxmega128A1

- Complete MMC firmware compatible to MMC V1.0. Firmware is fully functional. It is not necessary to change the firmware. However, C source code of this firmware is available;
- JTAG chain switching done inside firmware;
- HPM-based SPI firmware update included for fallback. (Provided PCIe-to-SPI programming core inside FPGA is recommended for fast flash update);
- Control over IPMI or UART via USB.

JTAG CPLD

- Complete MMC Firmware compatible to MMC V1.0. Firmware is fully functional. It is not necessary to change the firmware. However, VHDL source code of this firmware is available.

Transceiver FPGA

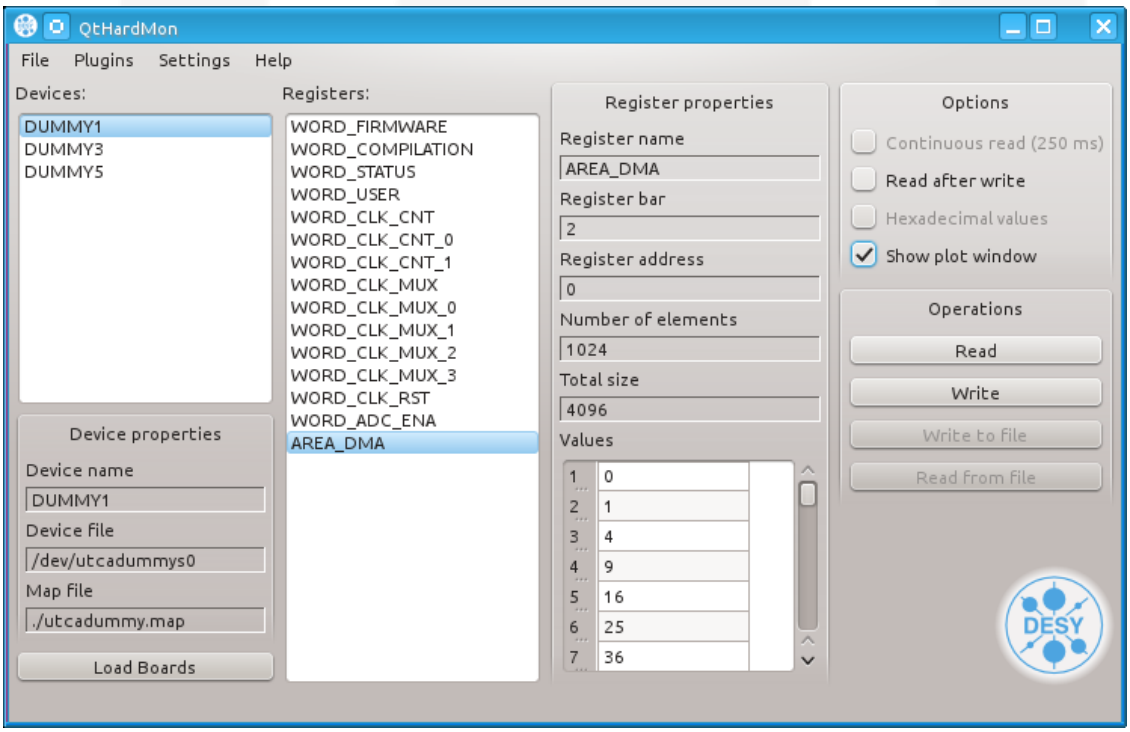
- SPI FLASH memories are pre-programmed with DAMC-FMC20 board support package (available as source code);
- PCIe-to-SPI programming is provided.

Main FPGA

- Platform FLASH contains board support package (available as source code) with demo application;
- Demo application allows reading and writing registers through transceiver FPGA via PCI express;
- Board support package and demo application is available as source code.

PC utilities (Linux)

- Firmware update utility (to update transceiver FPGA via PCIe-to-SPI) including JTAG player to update main FPGA Platform Flash);
- Easy graphical PCIe register read-and-write tool (MTCA4U), based on QT.



4. Technical Specifications

The main technical specifications for the **DAMC-FMC20** are presented in the following table:

Architecture			
Physical		*Dimensions*	Double width, Mid-Size with Full-Size option
			Width: 5.486" (148.5 mm)
			Depth: 7.110" (180.6 mm)
Standards		*AMC.0, AMC.1, AMC.2, MTCA.4*	Advanced Mezzaninice Card
		Module management	IPMI Version 2.0, MMC V1.0 compatible
Compatibility		*Zone3 classification*	Class D1.0
		Compatible AMC products	DRTM-VM2, TBD
Configuration			
Electrical properties		*Power consumption*	< 50 W
Connectivity			
Front Panel	*FMC slots*	*HPC*	1 slot
		LPC	1 slot
	Debug interface	*Front panel*	3 channel, booth FPGAs and MMC
		Connector type	Micro USB
		Data throughput	3 Mbps
Backplane	*Low latency connection*	*Backplane*	up to 2 channels
		Connector type	Peer-to-peer, ports 8-15 according to AMC spec.
		Data throughput	2.7 or 3.2 Gbps (depending on FPGA)
		Bit error rate	$< 10^{14}$ bit^{-1}
	PCIe	*Backplane*	1 lane
		Connector type	PCIe gen. 2.0
		Data throughput	2.5 Gbps
		Bit error rate	$< 10^{14}$ bit^{-1}
Zone 3	*Parallel bus*	*RTM*	53 differential pairs
		Connector type	LVDS

		Bit error rate	$< 10^{14}$ bit^{-1}
	Others	*MTCA.4 signals*	IPMI bus - I^2C, presence, power supply
		Interlocks	Dedicated output signals
		JTAG	JTAG chain, +3V3
Other Features			
On Board		*RTM management*	With power supply and current monitoring
		Firmware upgrade	Yes, via IPMI and PCIe interface
		Voltage and current monitor	Yes, readout via IPMI
		Clock monitoring	Yes, readout via IPMI
		LEDs	IPMI management control
		Mechanical	Hot swap ejector handle
Environmental		*Operating temperature*	0 – 45°C
		Storage temperature	-40 … 90°C
		Relative humidity	5 to 90%, non-condensing
		Weight	220 g

Table 3: Technical Specifications – **DAMC-FMC20**