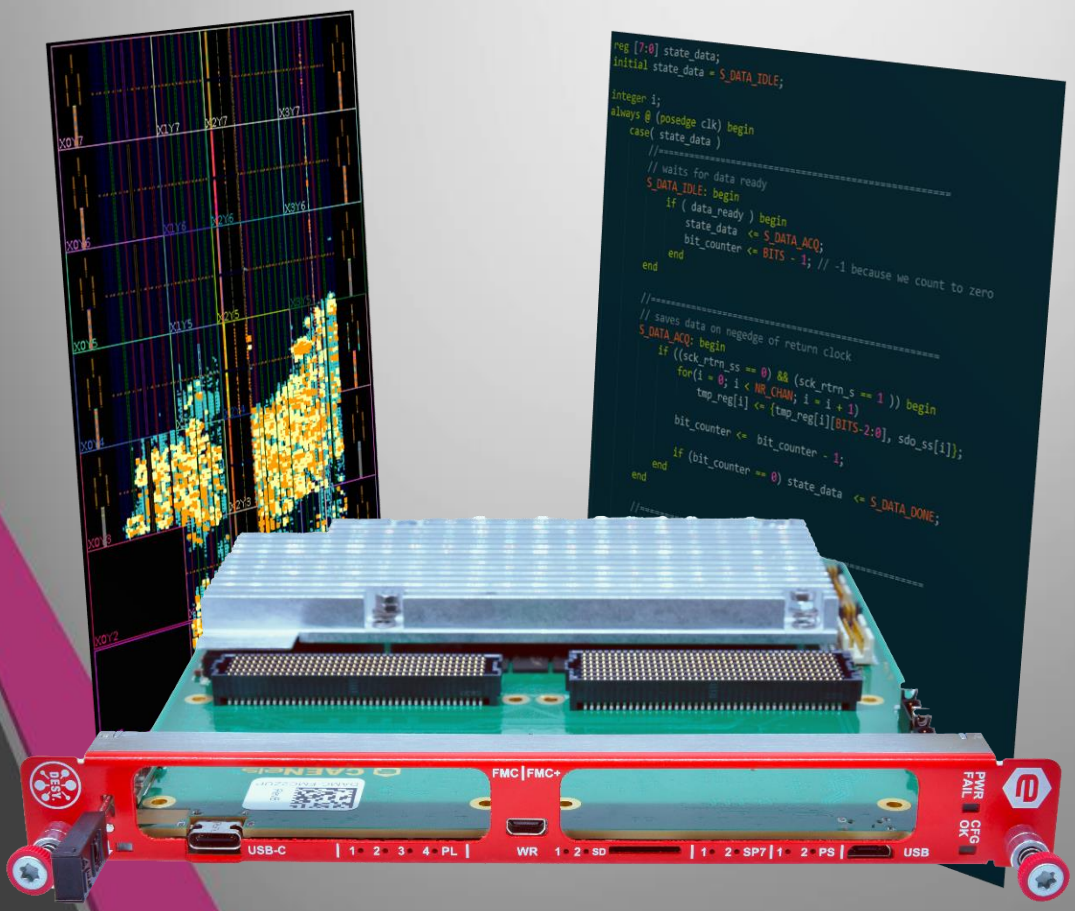
DAMC-FMC2ZUP

Zynq Ultrascale+ MPSoC based Dual FMC/FMC+ Carrier Board with MicroTCA.4 D1.1 support

CAENels
Gear For Science

User's Manual



MTCA.4 – MicroTCA for Physics

Rev.2 – August 2024

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Document Revisions

Document Revision	Date	Comment
Preliminary Release	October, 2020	Preliminary Release
1.0	April, 2021	First Release
1.1	May, 2023	Clock tree image updated. I2C bus description added. MMC command table updated.
1.2	January, 2024	Corrected image section FMC/FMC+ connections
2	August 8th2024	Updated address and revision numbering

Safety Information

The following table shows the general environmental requirements for a correct operation of referred board in this User's Manual:

Environmental Conditions	Requirements
Environment	Indoor use
Operating Temperature	0°C to 50°C
Operating Humidity	20% to 80% RH (non-condensing)
Altitude	Up to 2000 m
Pollution degree	2
Storage Temperature	-10°C to 60°C
Storage Humidity	5% to 90% RH (non-condensing)

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Please read carefully the manual before operating any part of the board.

1. Introduction

This chapter presents the overall characteristics and features of the DAMC-FMC2ZUP FMC carrier board.

1.1 DAMC-FMC2ZUP Description

The DAMC-FMC2ZUP is a high-end FMC/FMC+ carrier in MicroTCA.4 form factor based on the new family of ZYNQ Ultrascale+ MPSoCs. The host FPGA is the Xilinx ZU11EG-L2 or the ZU19EG-L2. The PS (Processing System) section offers a quad-core ARM Cortex-A53 operating up to 1.333 GHz, a dual core ARM-R5 real-time processor running up to 533 MHz and Mali-400 MP2 graphics up to 600 Mhz.

The board features extensive MicroTCA.4 backplane connectivity. PCI express Gen.3 x4 link is supported on port 4-7 and can be expanded to x8 using ports 8-11 in systems that support this mode of operation.

The card supports full multi-gigabit point-to-point link connectivity (low-latency links) on ports 12-15. This can eventually be expanded to include ports 8-11 (PCIe is restricted to x4 configuration in this use-case) to accommodate non-conventional backplane topologies.

Gigabit Ethernet port 0 is directly connected to the PS subsection of the FPGA while port 1 connects to the PL (Programmable Logic) MGTs to allow implementation of a SGMII interface over backplane.

Two transceivers from PS are connected to AMC port 2 and 3, allowing attachment of up to two standard off-the-shelf MicroTCA SATA cards with hard drives or SSDs.

All eight M-LVDS Timing/Trigger signals on ports 17-20 are accessible.

The four TCLK lines and the Fabric FCLKA are all connected to the internal clock distribution network. A flexible clock scheme leveraging a 16-channel bi-directional cross point switch allows to receive and/or drive any clock from/to the backplane (TCLKA, TLCKB, TCLKC, TCLKD) and from/to the FMCs (bi-directional clocks).

The board features two DDR4 interfaces, a 64-bits wide 4GB memory directly attached to the PS and a 16-bits wide 1GB memory connected to the PL, both memories operate by default at 2400 MT/s, with the option to increase the data-rate to 2666 MT/s for the PL when the board does not operate on low-power core voltage. The card

provides two FMC sockets, one FMC+ (VITA 57.4 compliant) and one FMC High Pin Count (VITA 57.1 compliant). Both connectors populate all LA and HA differential pair lines and can operate on VADJ level in the range from 1.2V to 1.8V. A total of 24 transceivers are routed to the FMC+ socket and 8 to the FMC HPC connector. Front panel connectivity comprises a Micro HDMI type-D connector with a proprietary pin assignment offering a Gigabit Ethernet interface (over external SFP), clock input and two trigger in/out signals. The front panel Gigabit Ethernet connection can be used in conjunction with the available HW infrastructure provided on the board to implement a White Rabbit endpoint.

A fully fledged USB Type-C connector implementing Alternate Mode Display Port is connected to the PS, this allows to provide USB HS, USB SS 3.0, DisplayPort and power delivery capabilities on a single compact interface. This offers the possibility to omit CPU boards in the MicroTCA system.

The RTM interface is designed according to class D1.1 and implements the full set of 42 LVDS lines and 2 MGT links. The board supports all existing digital RTMs from DESY (i.e. DRTM-AD84, DRTM-VM2, DRTM-PZT4).

The ARM Cortex-A53 processor in the MPSoC can run GNU/Linux from a MicroSD card on the front panel or from the embedded 8GB eMMC flash memory. The Zynq Ultrascale+ family of FPGAs is supported by all modern development tools, such as Vivado, HLS, Yocto, Petalinux, SDSoC and SDAccel, this makes DAMC-FMC2ZUP capable of addressing the ever-growing need of processing power while also reducing development time.

1.2 DAMC-FMC2ZUP Features

- Two FPGA Low-Power Xilinx MPSoC Ultrascale+ options are available:

MPSoC FPGA	ZU11EG-L2	ZU19EG-L2
Logic Cells	653 k	1.143 k
DSP Slices	2.928	1.968
BlockRAM	21.1 MiB	34.6 MiB
UltraRAM	22.5 MiB	36.0 MiB
PCIe	Gen. 3 x4 or x8	
Ethernet MAC	100G	
ARMs	1.333 GHz Quad-Core ARM Cortex-A53, MALI-400 GPU, 600 Mhz Dual-core ARM Cortex-R5	
GTY transceivers	16 GTY transceivers (28.21 Gbps) routed to FMC+ transceivers	

GTH Transceivers	32 GTH Transceivers (16.375 Gbps/ 12.5 Gbps) low-power) routed to FMC HPC, backplane, Front Panel, Zone3 etc.
GTR Transceivers	4 GTR Transceivers (6.0 Gbps) routed to SATA links and FMC connector

- FPGA core voltage can be set to low-power (0.72V) or standard power (0.85V) operation via MMC user commands, this allows to switch between low heat dissipation and higher performance
- FMC+ Slot providing 24 transceivers (16 GTY + 8 GTH) and full sets of LA and HA differential pairs
- Standard FMC HPC socket with 8 transceivers and full LA and HA connectivity
- USB Type-C connector providing DisplayPort and USB 3.0 interfaces. This allows to set-up a stand-alone system with display and USB host capability (may save a CPU module)
- Zone 3 Class D1.1 compliance with full interlock support
- 64-bit 4 GiB DDR4 with 2400 MT/s connected to PS (accessible from PL via AXI Bridge)
- 16-bit 1 GiB DDR4 with 2666 MT/s (2400 MT/s in low-power mode) connected to PL
- Flexible clock architecture provides access (receive/transmit) to all MicroTCA backplane clocks (TCLKA, TCLKB, TCLKC, TCLKD, FMC bidirectional clocks). 3 PLLs generate clocks for PS, Zone3 and FMCs
- White Rabbit Support (Input from front panel, output to backplane via M-LVDS and TCLKs)
- SD-Card slot (connected to PS) accessible from the front panel
- 8GB eMMC Memory
- Full MLVDS and interlock receive/transmit capability
- JTAG interface available from front panel accessible microUSB connector or AMC backplane (requires JSM module). FPGAs, FMCs and RTM can be set as target devices in the JTAG chain
- Full HPM update functionality

1.3 Ordering options

There are two ordering option for the two versions of the DAMC-FMC2ZUP carrier board:

Description	Ordering Code
MicroTCA.4 Zynq UltraScale+ FMC+ Carrier with **XCZU11EG--L2FFVC1760E**	DAMCFMC2ZUP1
MicroTCA.4 Zynq UltraScale+ FMC+ Carrier with **XCZU19EG--L2FFVC1760E**	DAMCFMC2ZUP2

1.4 DAMC-FMC2ZUP Components Overview

This section details the type and location of components on the board.

Components on side #1 (top-side):

1. Main FPGA - Zynq Ultrascale+
2. FMC+ connector
3. FMC HPC connector
4. Secondary FPGA Spartan 7
5. DDR4 memory modules, PS (a), PL (b)
6. Power Section
7. Ethernet IC
8. Main JTAG Connector
9. FPGA PS - ARM JTAG for PS Connector
10. Extension Power Connectors

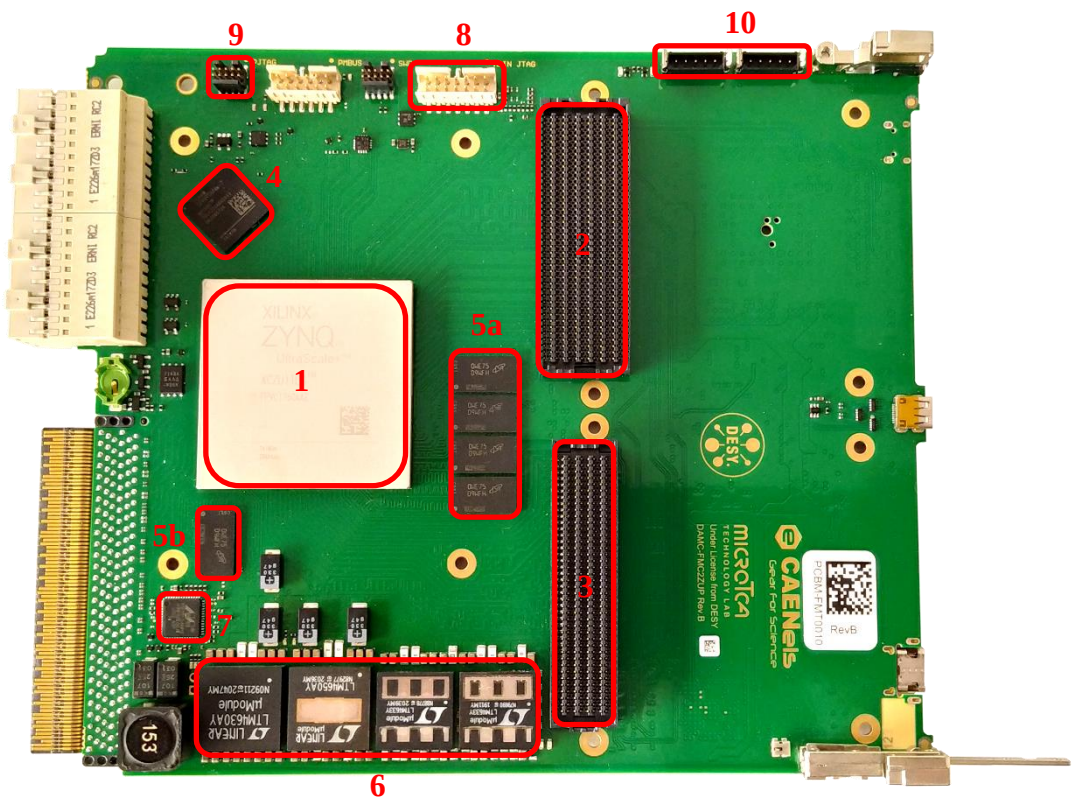


Figure 1-1: DAMC-FMC2ZUP - Top side

Components on side #2 (bottom-side):

1. MMC
2. MLVDS transceivers
3. Flash memories for FPGA configuration:
    a. Zynq Ultrascale+
    b. Spartan 7
4. Power Management
5. Clock Section
6. eMMC memory

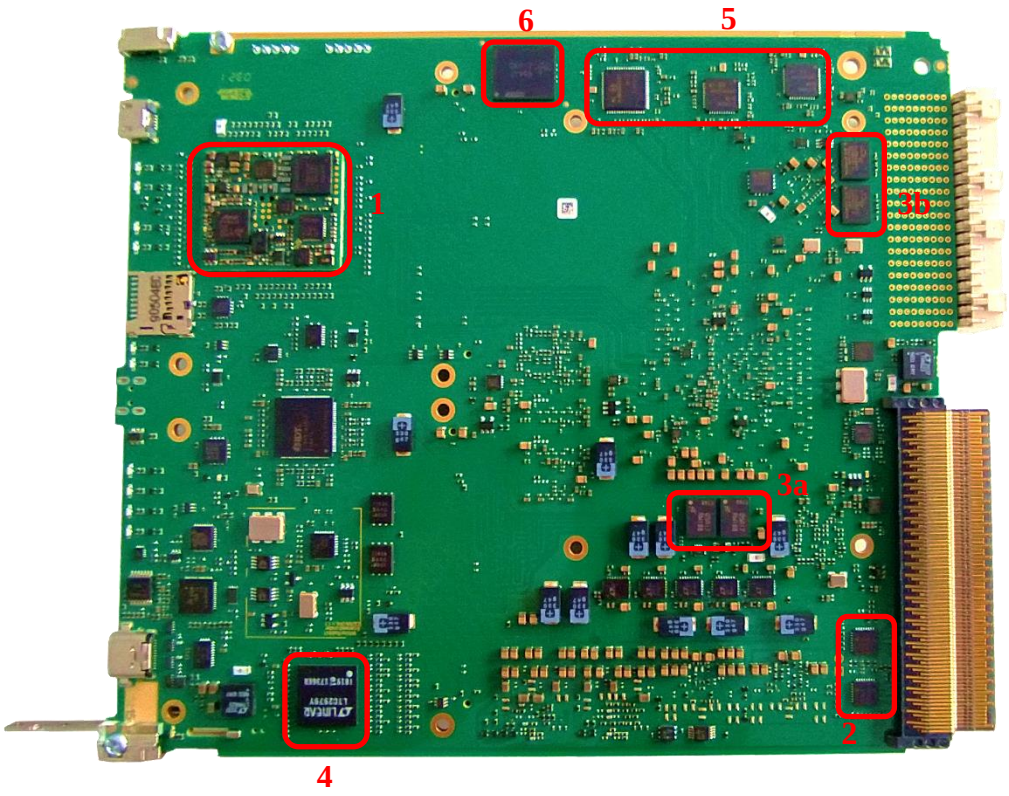


Figure 1-2: DAMC-FMC2ZUP - Bottom side

2. DAMC-FMC2ZUP Architecture

This chapter offers a technical overview of the many features implemented on this board.

2.1 Functional Block Diagram

This section presents the block diagram of the connectivity implemented on the board, excluding the clock network which is described in the next section. In the following paragraphs are described the connections with the backplane, with FMC/FMC+ connectors and with Zone3.

2.1.1 MicroTCA backplane

The following interconnections are available over the MicroTCA backplane:

Gigabit Ethernet (ports 0 and 1):

GbE interface on Port 0 is provided through a specialized RGMII to Ethernet 1000-baseX IC to guarantee fully compliance to the MicroTCA standard. The RGMII communication is under control of the PS, thus allowing an easy implementation of the required protocol stacks in software. The redundant GbE interface on Port 1 is connected to Multi-Gigabit Transceiver (MGT) on the PL and can be used as a SGMII interface to communicate with the redundant MCH.

SATA (ports 2 and 3):

Serial-ATA interfaces are directly connected to the PS MGTs. This gives the user flexibility to store data from an Operating System running on the ARM Cores to a Hard Disk Drive (HDD) or Solid-State Disk (SSD) residing on another AMC card. For further details on this interface please refer to the backplane connectivity manual.

PCIe over Fat Pipe (ports 4 to 7):

PCIe x4 Gen.3 (Gen.4 can be enabled but is not officially supported) connectivity is achieved using the Hard IP blocks located in the PL area of the FPGA. Connecting these ports to the PL MGTs instead of the PS ones offer many benefits among which a higher data throughput (PS MGTs are limited to PCIe Gen.2). This interface can be expanded to provide a x8 lanes link when ports 4 to 11 (Fat Pipe and Extended Fat Pipe) are used in systems that support this configuration[1].

Extended Fat Pipe (ports 8 to 11):

Ports 8 to 11 are routed to a dedicated MGT Quad on the PL section of the FPGA. These lanes can be used to extend the PCIe interface or to implement any other supported protocol (restrictions may apply depending on MicroTCA system configuration).

Low Latency Links (ports 12 to 15):

As for the previous link these ports are also routed to a dedicated MGT Quad of the PL. These lanes are usually implemented on the MicroTCA backplane as board-to-board links and their usage is user's application dependent.

M-LVDS (ports 17 to 20):

Ports 17 to 20 are implemented using specialized ICs and are accessible from the PL section of the Main FPGA. The enable signal of the transmitters is under control of the FPGA itself (optional factory configuration where RX19, TX19 and RX20 transmitters are always disabled). Read-back of the MLVDS lanes is always enabled and available to the FPGA logic.

[1] x8 links are not possible on systems with redundant MCHs due to the non-transparent nature of the PCIe switches in the bus enumeration process

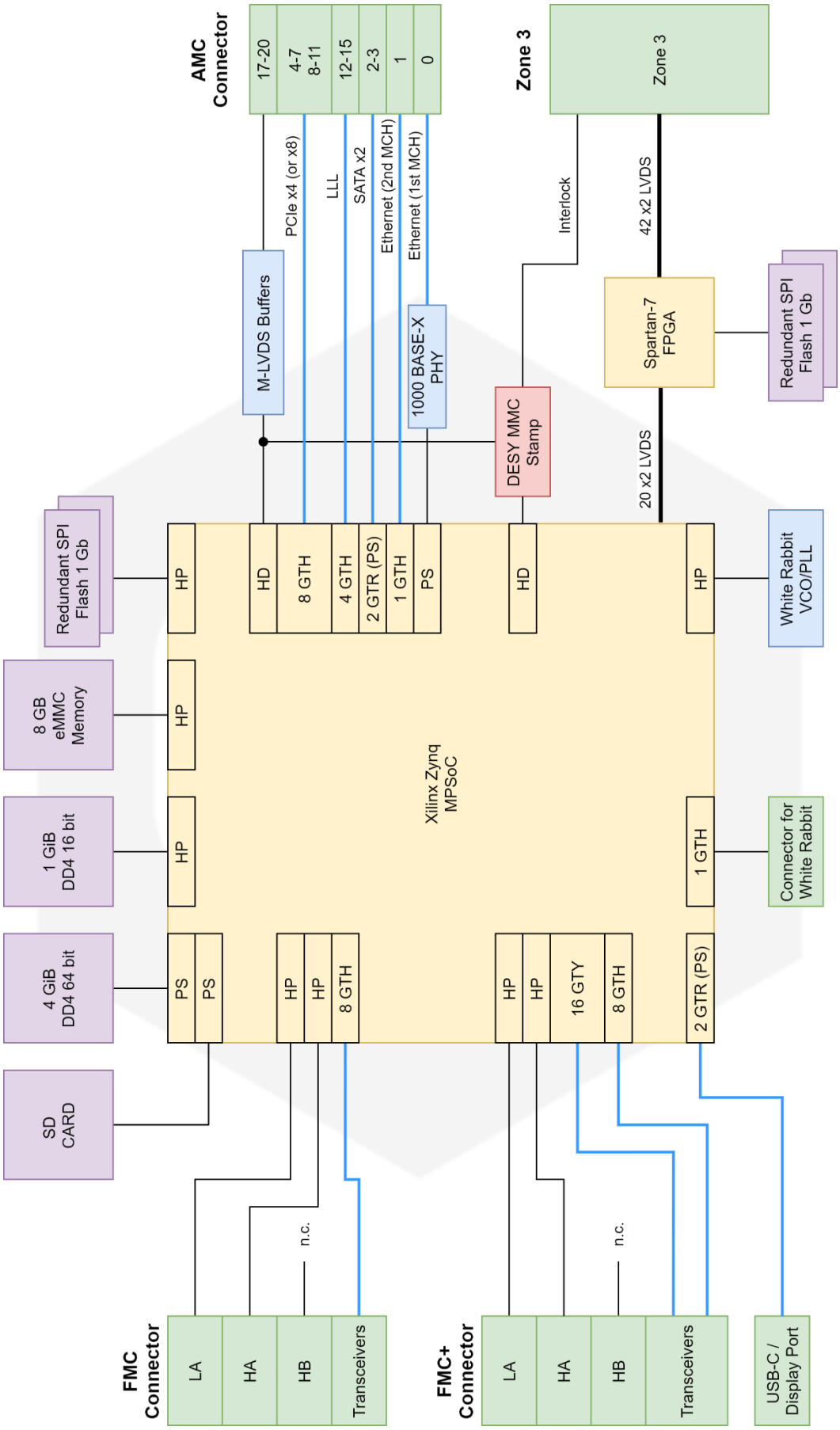


Figure 2-1: Block Diagram

2.1.2 FMC+ (VITA 57.4)

The following interconnections are available over the FMC+ connector:

- ***LA (00-33) LVDS Differential pairs:***

All the LA signals of the FMC interface are routed to the PL section of the FPGA. Two FPGA banks are associated to this interface, LA-00 to LA-16 are connected to one bank while LA-17 to LA-33 are routed to the other. LA-00, LA-01, LA-17 and LA-18 are clock capable pins routed to dedicated inputs on the FPGA, these signals have access to the clock resources on the PL.

- ***HA (00-23) LVDS Differential pairs:***

All the HA signals of the FMC interface are routed to the PL section of the FPGA. All the signals reside on the same I/O bank, HA-00, HA-01 and HA-17 are clock capable pins and are routed to dedicated inputs on the FPGA allowing them to access the clock resources of the PL.

- ***MGT interfaces:***

A total of 24 MGT (6 full MGT Quads) are provided to the FMC connector. 16 GTY Transceivers up to 28.21 Gb/s and 8 GTH Transceivers up to 16.375 Gb/s or 12.5 Gb/s (low power mode).

- ***CLK0-M2C and CLK1-M2C:***

Both signals are available and connected on dedicated clock input resources on the PL section of the FPGA. CLK0 resides in the same I/O bank as LA-00 to LA-16 and CLK1 resides in the same I/O bank as LA-17 to LA-33.

- ***GBT-CLK0, GBT-CLK1 and GBT-CLKHS 2 to 5:***

All signals are available and connected to the dedicated reference clock input resources of the associated PL MGT Quads. CLK0 resides in the same Quad as MGT lanes 0 to 3 and CLK1 resides in the same Quad as MGT lanes 4 to 7, CLKHS2 resides in the same Quad as MGT lanes 8 to 11 and so on.

2.1.3 FMC HPC (VITA 57.1)

The following interconnections are available over the FMC connector:

- ***LA (00-33) LVDS Differential pairs:***

All the LA signals of the FMC interface are routed to the PL section of the FPGA. Two FPGA banks are associated to this interface, LA-00 to LA-16 are connected to one bank while LA-17 to LA-33 are routed to the other. LA-00 and LA-17 are clock capable pins routed to dedicated inputs on the FPGA, this gives them access to the clock resources on the PL.

- ***HA (00-23) LVDS Differential pairs***:

All the HA signals of the FMC interface are routed to the PL section of the FPGA. All the signals reside on the same I/O bank, HA-00, HA-01 and HA-17 are clock capable pins and are routed to dedicated inputs on the FPGA, giving them access to the clock resources of the PL.

- ***MGT interfaces:***

A total of 8 GTH MGTs (two full MGT Quads) are available on the FMC connector.

- ***CLK0-M2C and CLK1-M2C***:

Both signals are available and connected on dedicated clock input resources on the PL section of the FPGA. CLK0 resides in the same I/O bank as LA-00 to LA-16 and CLK1 resides in the same I/O bank as LA-17 to LA-33.

- ***GBT-CLK0 and GBT-CLK1:***

Both signals are available and connected to the dedicated reference clock input resources on the PL MGT Quads. CLK0 resides in the same Quad as MGT lanes 0 to 3 and CLK1 resides in the same Quad as MGT lanes 4 to 7.

2.1.4 Zone3 Connectivity

Zone3 connectivity in accordance to recommended pinout of Class D1.1 is achieved as follows:

- **Fixed LVDS outputs OUT0 to OUT2:**

These links use specialized LVCMOS to LVDS drivers under full control of MMC Stamp SoM (System on Module). The driving signals are provided by the CPLD embedded on the MMC module.

- **AMC TCLK and CLK1:**

These signals are driven by the clock network as will be described in Section 2.2. To comply the unpowered/unconnected interface requirements described in the recommendation document, a LVDS buffer is used on both signal paths. The MMC has control over the enable signal of these buffers as required by the eKeying process.

- **RTM CLK1:**

This signal is driven by the RTM module and fed to the clock network as will be described in Section 2.2.

- **GTP0-1_CLK_IN and GTP0-1_CLK_OUT:**

Transceiver reference clocks from/to the RTM are part of the clock distribution network and described in Section 2.2.

- **GTP0 and GTP1 TX and RX pairs:**

High speed transceiver lanes are routed to dedicated TX and RX interfaces on a PL MGT Quad. This Quad is shared by the MGTs routed to the port 1 of the MicroTCA backplane and to the Micro HDMI type D connector on the front panel.

- **LVDS I/O differential pairs:**

A total of 24 LVDS pairs are available for user defined application on the Zone3 connector, these signals are routed to the Spartan 7 FPGA and from there, with a proprietary interface, to the main FPGA. This arrangement allows to interface to a RTM card whose logic levels are 2.5V.

- **Zone3 Management and Debug:**

Presence, I2C bus and JTAG signals are routed to the MMC Stamp SoM.

2.2 Clock Tree Architecture

The clock architecture is based on a bidirectional cross-point switch and 3 independent PLLs.

The cross-point switch is connected to:

- 4 Telecommunication Clock signals (TCLKA, TCLKB, TCLKC and TCLKD) provided on standard MicroTCA backplanes
- 3 digital clocks to and from the Zone3 connector
- the 2 bidirectional clocks of each FMC modules (CLKBIDIR2/3)
- one of the output clocks of the White Rabbit section
- FPGA I/O pins with dedicated access to internal clock tree resources
- the main PLL located on the board.

The board is capable of driving and receiving clock signals from any of the 4 TCLK dedicated paths of the MicroTCA backplane and from the bidirectional clocks of FMCs. The main PLL IC receives one input clock from the cross-point switch and provides one of its outputs back to it. The second input of this component can be externally provided through the Micro HDMI type D connector. Two of main PLL output are routed to the inputs of the 2 secondary PLL, used to fed the PS on the Main FPGA, and to the PLL towards the Zone3 connector. The other outputs are used as reference for MGTs and to synchronize the PL section of the Main FPGA.

The secondary PLL listed as PS PLL in the previous block diagram is responsible to provide the needed reference clocks to PS section of the Main FPGA. Any modification in the register values of this component might impact negatively the performances of the PS and in some cases prevent the ARM cores from booting up.

The Zone3 PLL provides the RTM related clocks and synchronization between the secondary FPGA (Spartan 7) and Main FPGA to ensure the proper functionality of the interconnection bus. The Fabric Clock (FCLKA) distributed by the MCH in a MicroTCA system is connected, through a PCIe compliant jitter cleaner IC, to a reference clock input of the MGT Quad used to implement the PCIe connectivity on ports 4-7. Fixed frequency clock resources are connected to various components to ensure proper operation and availability of a reference signal to the programmable logic even before the local PLLs are accessed and configured by the user code.

The PLLs are accessible over an I2C bus by both the MMC Stamp SoM and Main FPGA PS.

The block diagram of the clock network is presented in the following figure:

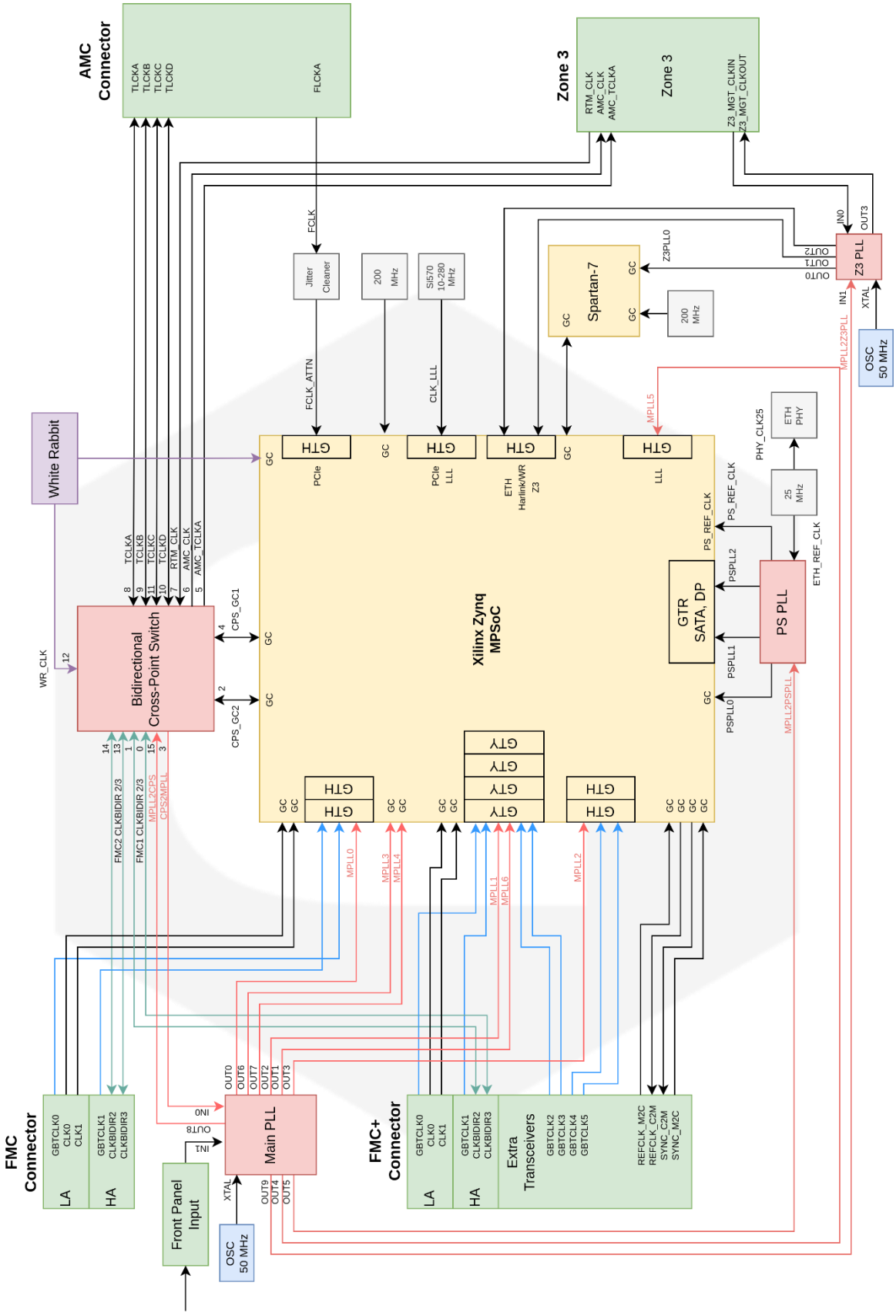


Figure 2-2: Clock Network Diagram

2.3 I2C Bus Addressing

2.3.1 CLOCK I2C BUS

Address	Device
0x50	EEPROM+MAC
0x55	LLL Clock Oscillator (Si570)
0x58	Clock CPS (Cross-point Switch)
0x70	MUX on MMC Stamp
0x71	MUX on Carrier (PCA9545A)
0x75	S7/Zone3 PLL (SI530A)
0x76	PS PLL (SI530A)
0x77	Main PLL (SI5341A)

Table 1: CLOCK I2C bus

Half of the EEPROM on the CLOCK I2C bus at address 0x50 is available to the application to store any data that's necessary for the operation (e.g. serial number, calibration date, calibration coefficients) while the second half is write protected and contains the factory configured unique ID (UID) which is used as MAC address.
The LLL Clock Oscillator on address 0x55 drives the MGTREFCLK1 on GTH bank 226. This clock can be used to clock the transceivers on the backplane connections and also the adjacent transceiver banks.
The CPS (Cross-Point Switch) on address 0x58 can route clocks to different parts of the board. For example, it can drive the TCLKx inputs to the other parts of the board and also the other way around.
For more information about the CPS and the PLLs see the BSP User Manual.

2.3.2 CONFIG I2C BUS

Address	Device
0x20	Expander Carrier Mode Switches
0x21	Expander FMC Status
0x70	MUX on MMC Stamp
0x71	MUX on Carrier

Table 2: CONFIG I2C bus

2.3.3 FMCx I2C BUS

Address	Device
0x50	FMC1 EEPROM
0x52	FMC2 EEPROM
0x70	MUX on MMC Stamp
0x71	MUX on Carrier

Table 3: FMCx I2C bus

2.3.4 SENS I2C BUS

Address	Device
0x18	FPGA Temperature Sensor
0x48	MMC Stamp Temperature Sensor
0x49	Inlet Temperature Sensor
0x4A	Outlet Temperature Sensor
0x4B	LTM Temperature Sensor

Table 4: SENS I2C bus

2.4 Power Supply Architecture

The power supply section is implemented by a cascade of DC/DC converters and LDOs, all of which are controlled by a PMBus manager IC, this ensures that the proper sequencing, as required by the FPGA and IC specifications, is maintained both at start-up and power-down. The PMBus manager offers full telemetry and monitoring of the power rails (voltage and current readouts) and is responsible to bring the board to a safe condition whenever a supply voltage is out of specifications.

This component also allows trimming the output voltages and it's responsible to set the VADJ rail to the voltage level required by the FMC modules. The MMC Stamp SoM has full control over the power conversion stages through the PMBus manager. By interfacing to the MCH the user can access the readout values for the following power rails:

- 0.72/0.85 V Main FPGA Core
- 1.0 V Secondary FPGA Core
- TBD

A general overview of the power section is presented in Figure 2.3.

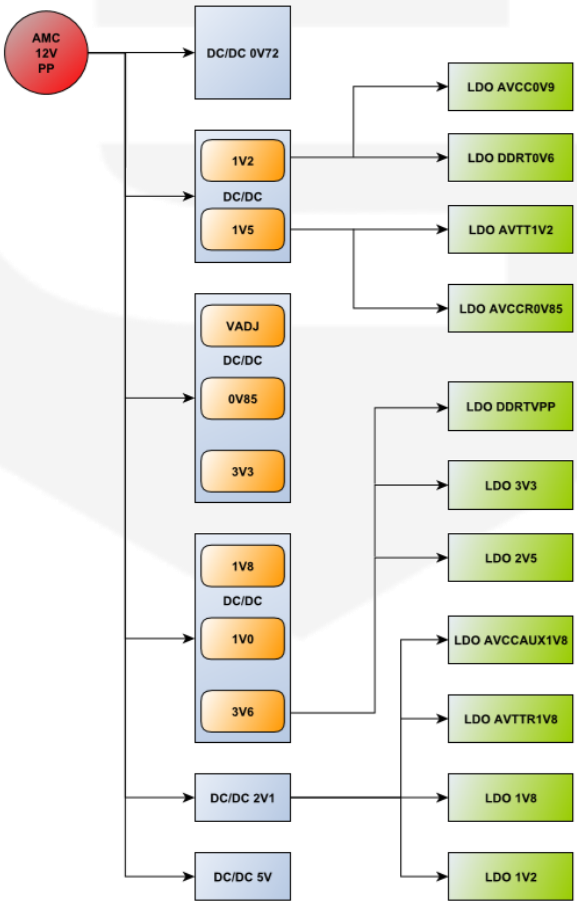


Figure 2-3: Power-Supply Section

2.5 JTAG Chain

The board implements two, not fully independent, JTAG chains. The main JTAG chain can be accessed through the P1 Connector (see Figure 1-1 for location on board) or the MicroTCA backplane and is "mediated" by the MMC Stamp SoM. The MMC Stamp is responsible to select and/or insert more devices into the JTAG chain. The connected devices are:

- Main FPGA PS JTAG Interface with all internal Controllers accessible by default (refer to Xilinx UG1085 Zynq UltraScale+ Device TRM Chapter 39 Figure 39-1)
- Secondary FPGA JTAG Interface
- FMC and FMC+ connectors JTAG signals
- RTM JTAG chain

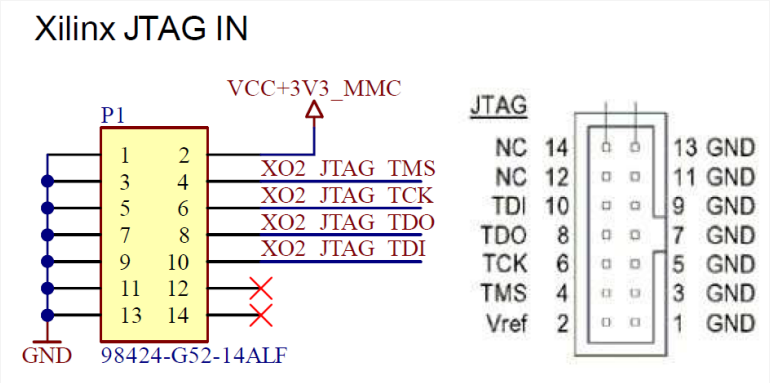


Figure 2-4: Main JTAG chain

The second JTAG chain is accessible from Connector P4 (see Figure 1-1 for location on board) and includes only the Main FPGA Arm DAP Controller to facilitate the software development on the PS of the Zynq ARM CPUs (refer to Xilinx UG1085 Zynq UltraScale+ Device TRM Chapter 39, PJTAG/Arm DAP Sections) by providing a dedicated debug interface.

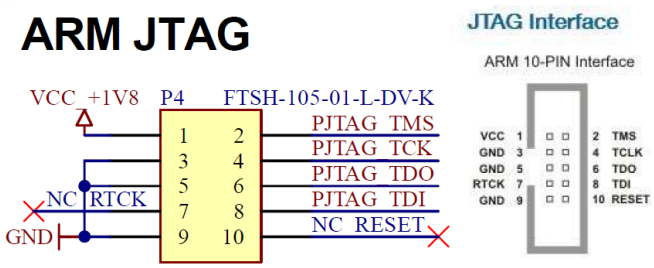


Figure 2-5: ARM JTAG

2.6 FLASH Programming

In addition to the microSD card available on the front panel and the embedded eMMC (not supported as primary boot device in the design) the board hosts 2 redundant sets of serial flash memories. One set is dedicated to the Main FPGA (Zynq Ultrascale+) and one to the secondary FPGA (Spartan 7). The selection of which of the 2 devices available for each FPGA will be used during the configuration process is controlled by the MMC Stamp SoM (see FPGA boot mode selection). The Flash memories can be accessed through the same device they will program using the JTAG interface and a supported programming device/tool connected to the on-board JTAG connector or MicroTCA JSM (JTAG Switching Module) or they can be accessed for in-chassis programming by the MMC Stamp through IPMI instructions (HPM.1, Hardware Platform Management).

2.7 White Rabbit Support

The board provides most of the necessary infrastructure needed to implement a White Rabbit End Point. The interconnections required to implement the missing features are made available on the front panel high density connector whose pin-out is described in section 5.6). A breakout board with an SFP/SFP+ interface has to be connected to the high-density connector to complete the set of required components of a White Rabbit endpoint. Alternatively, port 1 on the MicroTCA backplane could be used for this purpose although this is not the preferred method and might require an additional MCH.

The firmware needed to operate the White Rabbit End point on the DAMC-FMC2ZUP can be derived from the OpenHardware Cute-WR project (information available on ohwr.org). The firmware customization required will later on be made available under the OpenHardware license terms.

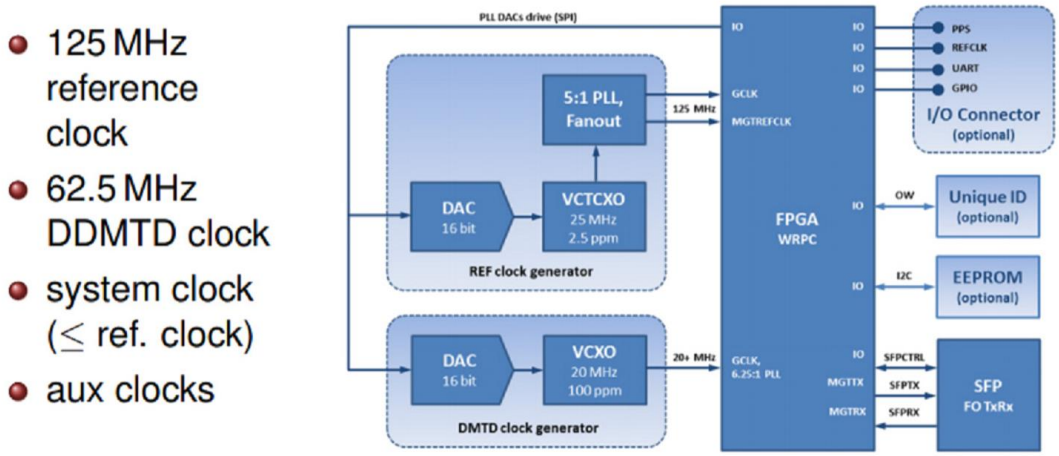


Figure 2-6: Block Diagram of DAMC-FMC2ZUP White Rabbit Section

3. Module Management Controller

The MMC Stamp SoM implements standard MicroTCA module management as well as the following additional features:

- JTAG multiplexing
- HPM update
- Boot mode selection for both ZUP and Spartan-7 FPGAs
- Interlock multiplexing
- Auto-detection of variable FMC voltage (Vadj)

3.1 Serial Console

The MMC Stamp implements a command line interface on a serial port that's forwarded to the front panel USB connector. It uses VT100 escape sequences to support convenience features like colors, autocompletion and shell history. To avoid flooding "dumb" terminals with unsupported escape sequences, a fallback dumb terminal mode is supported as well. This chapter lists some example commands, for a full list see MMC command list.

3.2 JTAG multiplexing

The JTAG interface can be multiplexed between different sources and targets. The JTAG signals on the on-board connector or the backplane can be routed to the ZUP, the Spartan-7, the first or secondary FMC slot or the RTM.

Example command:
`sj bp fpga1` will route JTAG from the backplane to the main FPGA.

3.3 HPM update

The MMC Stamp currently supports in-application-update of its firmware using the PICMG HPM.1 standard. Upcoming MMC firmware releases will also be able to update FPGA images.

The firmware upgrade can be done with ipmitool using a command like this:

```
ipmitool -H <mch_address> -B 0 -b 7 -T 0x82 -t <amc_ipmb_address> hpm upgrade
/path/to/firmware.hpm
```

3.4 XMODEM update

For situations where update through IPMI is not viable, all available HPM targets can also be updated via XMODEM over the serial USB. The update has to be initiated with the `xm` console command.

3.5 FPGA boot mode selection

The ZUP boot mode can be set to JTAG, first or secondary flash, SD card or PJTAG. The Spartan-7 boot mode can be set to JTAG, first or secondary flash.

Example commands:

`bz sd` will configure the ZUP to boot from SD card;
`b7 spi2` will configure the Spartan-7 to boot from the secondary SPI flash;
`rz will` reconfigure the ZUP;
`r7` will reconfigure the Spartan-7.

3.6 Interlock multiplexing

The interlocks can be multiplexed between sources rx19, tx19, rx20, zup and targets out0, out1, out2.

Example command:
`ci out1 tx19` will route interlock TX19 to interlock out1.

3.7 Auto-detection of variable FMC voltage (Vadj)

The VCC_Vadj power rail towards the FMC slots can be adjusted within the limits allowed for the ZUP's I/Os. The MMC supports detection of the FMC module's supported voltage range (by reading out the DCLoad FRU record of the Vadj channel) and automatic setting of a suitable level for Vadj.

If autodetection fails, a manual setting of Vadj level has to be configured.

Example commands:
`fmv 1.4` will set the Vadj level to 1.4 volts;
`fmv auto` will set the Vadj level to auto-detect.

3.8 RTM e-keying

RTMs are compatibility-checked according to the MicroTCA 4.1 standard. The RTM's FRU is searched for a Zone3 Compatibility Record matching the AMC, and payload power to the AMC is only enabled if a matching record is found. For RTMs with an invalid FRU or missing Zone3 Compatibility Record, this check can be manually overridden.

Example commands:
`rte enable` will enable the RTM compatibility check (default).
`rte override` will disable / override the RTM compatibility check.

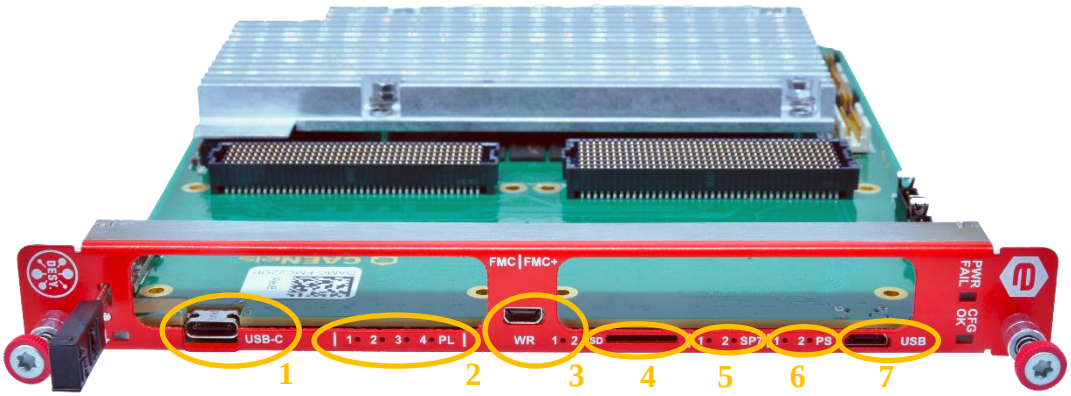
3.9 RTM temperature sensors

The MMC supports up to four MAX6626 temperature sensors on the RTM at the I2C addresses 0x48-0x4b. The command `st` sets a bitmask enabling a set of these four possible sensors.

Example commands:
`st 0` will disable all RTM temperature sensors.
`st 5` will enable RTM sensors 1 and 3 at 0x48 and 0x4a.

4. Front Panel Available Features

The board provides many features accessible from the front panel, as shown in the following figure:



Section	Description
1	USB Type-C connector: USB2, USB3 and DisplayPort are available on this interface
2	User accessible LEDs from Main FPGA PL
3	High Density microHDMI type-D with proprietary pinout for White Rabbit with 2 leds
4	microSD slot. Can be used to expand storage capabilities and/or used to provide a rootfs and OS to Main FPGA PS
5	Secondary FPGA (Spartan7) status LEDs
6	User accessible LEDs from Main FPGA PS
7	microUSB connector: provides access to MMC Stamp and Main FPGA PS system console

Figure 4-1: Front Panel

4.1 microUSB Front-panel Connector

The microUSB front panel connector allows access to:

- MMC Stamp and
- Main FPGA PS

consoles from an external PC.

On Windows™ systems, when an USB cable is connected to this interface, 2 new COM peripherals will be detected. To identify the number associated to these peripherals refer to the "Device Manager Tool" provided by the Windows™ OS.

On Linux based operating systems, when an USB cable is connected to this interface, 2 new devices will appear into the `/dev/` folder, usually they are identified as "`tty`" devices. Monitoring the output of the `dmesg` command upon connection of the board might help to identify the proper device names.

The consoles can be accessed with tools like Putty or minicom with the following configuration:

Configuration	Value
Baudrate	115200
Data bits	8
Stop bits	1
Parity	None
Flow control	None

Figure 4-2: MMC UART configuration

Configuration	Value
Baudrate	115200
Data bits	8
Stop bits	1
Parity	None
Flow control	XON/XOFF

Figure 4-3: MAIN FPGA UART configuration

5. Appendix

5.1 Extension Power Connectors

The following figure defines the pin assignment of the 2 Extension Power Connectors available on the board (see Figure 1-1: DAMC-FMC2ZUP - Top side)

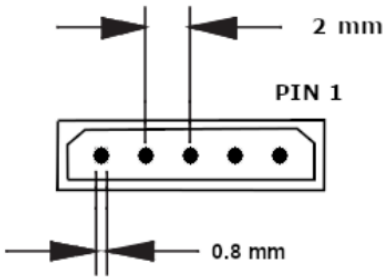


Figure 5-1: Pin allocation of Extension Power Connectors

Pins 1, 3 and 5 are connected to VCC12_FMC, a 12V power rail available whenever the FMC power is enabled on the regular connectors. Pins 2 and 4 are connected to GND.

5.2 Backplane Assignments

PORT	FUNCTION	NAME	ASSIGNMENT
0	1 GbE	TRX0	PHY (MIO)
1	1 GbE	TRX1	GTH
2	SATA	SATA.CH0	MGTR
3	SATA	SATA.CH1	MGTR
4	PCIe	PCIE1	GTH
5	PCIe	PCIE2	GTH
6	PCIe	PCIE3	GTH
7	PCIe	PCIE4	GTH
8	PCIe/LLL	LLB.CH8	GTH
9	PCIe/LLL	LLB.CH9	GTH
10	PCIe/LLL	LLB.CH10	GTH
11	PCIe/LLL	LLB.CH11	GTH
12		LLC.CH12	GTH
13		LLC.CH13	GTH
14		LLC.CH14	GTH
15		LLC.CH15	GTH
16	TCLKC/D	TCLKC/D	CPS
17	MLVDS	MLVDS.TRX17	MLVDS transceiver
18	MLVDS	MLVDS.TRX18	MLVDS transceiver
19	MLVDS	MLVDS.TRX19	MLVDS transceiver
20	MLVDS	MLVDS.TRX20	MLVDS transceiver
CLK1	TCLKA	TCLKA	CPS
CLK2	TCLKB	TCLKB	CPS
CLK3	FCLKA	FCLK	Jitter Cleaner

Table 5: Backplane assignments

5.3 PCIe Assignments (x4)

PCIe 4-7	FPGA pin (Bank 228, GTH)
PCIE4_RX_N	AD3
PCIE4_RX_P	AD4
PCIE4_TX_N	AC5
PCIE4_TX_P	AC6
PCIE3_RX_N	AC1
PCIE3_RX_P	AC2
PCIE3_TX_N	AB7
PCIE3_TX_P	AB8
PCIE2_RX_N	AB3
PCIE2_RX_P	AB4
PCIE2_TX_N	AA5
PCIE2_TX_P	AA6
PCIE1_RX_N	AA1
PCIE1_RX_P	AA2
PCIE1_TX_N	Y7
PCIE1_TX_P	Y8
CLK_N	AB11
CLK_P	AB12

5.4 PCIe Assignments (x8)

PCIe 8-11	FPGA pin (Bank 227, GTH)
CH11_RX_N	AH3
CH11_RX_P	AH4
CH11_TX_N	AG5
CH11_TX_P	AG6
CH10_RX_N	AG1
CH10_RX_P	AG2
CH10_TX_N	AF7
CH10_TX_P	AF8
CH9_RX_N	AF3
CH9_RX_P	AF4
CH9_TX_N	AE5
CH9_TX_P	AE6
CH8_RX_N	AE1
CH8_RX_P	AE2
CH8_TX_N	AD7
CH8_TX_P	AD8
CLK_N	AD11
CLK_P	AD12

5.5 MLVDS Assignments

MLVDS	FPGA pin (Bank 88, HD 3V3)
RX20_TX	N11
RX20_RX	M12
RX20_TXEN	J12
TX20_TX	N10
TX20_RX	M11
TX20_TXEN	K10
RX19_TX	M13
RX19_RX	L13
RX19_TXEN	K11
TX19_TX	L12
TX19_RX	N12
TX19_TXEN	L10
RX18_TX	P12
RX18_RX	P14
RX18_TXEN	J13
TX18_TX	K12
TX18_RX	R14
TX18_TXEN	M10
RX17_TX	P13
RX17_RX	L14
RX17_TXEN	J14
TX17_TX	N13
TX17_RX	N14
TX17_TXEN	K14

5.6 High Density microHDMI type-D

On the front panel it is also present a High Density microHDMI connector (type-D) that can be used for trigger/clock/white-rabbit purposes. The block diagram of the available connections is shown in the following figure:

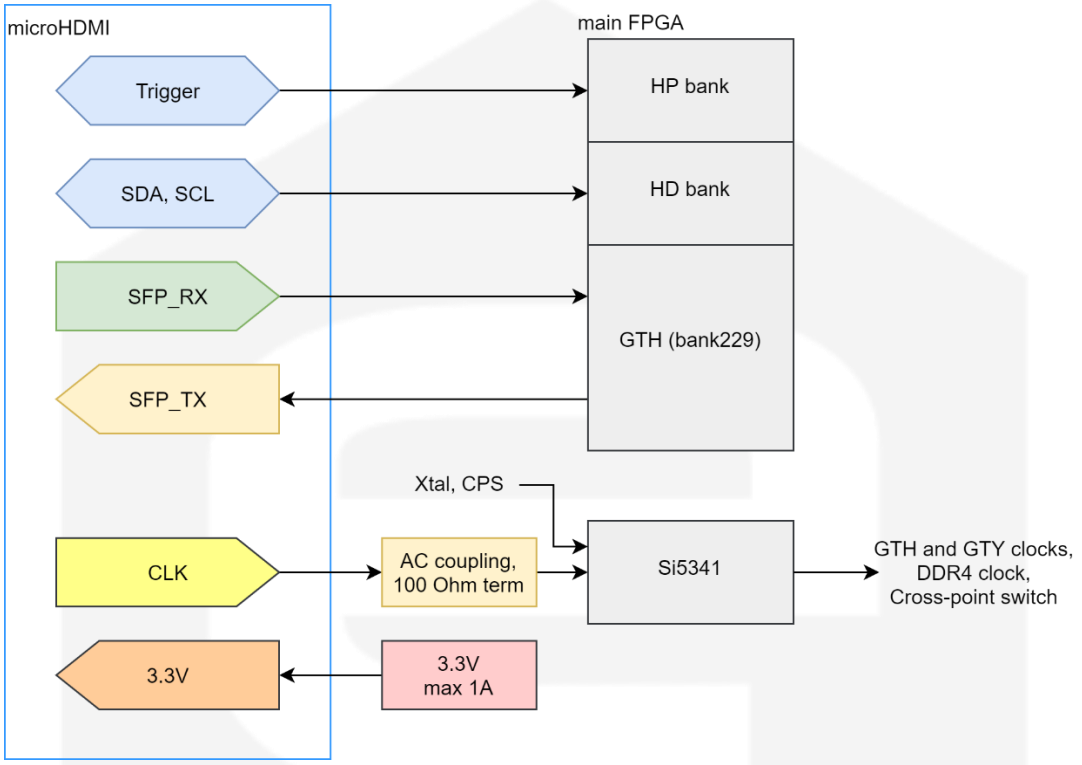
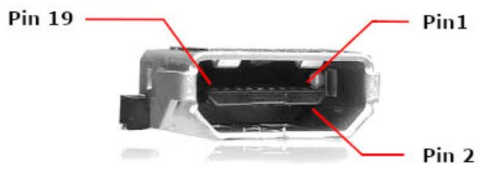


Figure 5-2: Block Diagram of the microHDMI connections

The microHDMI pin connections of connector are listed in the following table:



Name	Pin #	Type
TRIGGER_1_N	1	LVDS 2V5 INOUT
TRIGGER_1_P	2	LVDS 2V5 INOUT
TRIGGER_0_P	3	LVDS 2V5 INOUT
GND	4	PASSIVE
TRIGGER_0_N	5	LVDS 2V5 INOUT
SFP_TX_P	6	MGT
GND	7	PASSIVE
SFP_TX_N	8	MGT
SFP_RX_P	9	MGT
GND	10	PASSIVE
SFP_RX_N	11	MGT
CLK_IN_P	12	CLK INPUT
GND	13	PASSIVE
CLK_IN_N	14	CLK INPUT
3V3	15	PASSIVE
GND	16	PASSIVE
SCL	17	3V3 LVCMOS OUT
SDA	18	3V3 LVCMOS INOUT
3V3	19	PASSIVE

Figure 5-3: High Density microHDMI pins connections

Trigger signals can be used to provide an external trigger to the Main FPGA or to send such signal from the board to another device. Trigger signals on the connector are differential LVDS and must not reach a level higher than 2.5V referenced to board logic ground under any circumstance, failure to adhere to this requirement might result in permanent damage.

CLK_IN signal is an LVDS compliant input with maximum input frequency of 200MHz, the highest voltage level allowed by the interface that does not result in damage is 4V.

SFP_TX/RX are high speed transceivers provided to connect to an external SFP/SFP+ module or another long-range high-speed interface.

MGT interface can be used to connect to a White Rabbit enabled network.

3V3 is connected to the board local 3.3V supply rail and can be used to power an external SFP/SFP+ module.

The pin assignments are listed in the following table:

Name	Component	Pin #	Bank Voltage	Notes
TRIGGER_1_N	Main FPGA	F20	FMC1 Vadj	
TRIGGER_1_P	Main FPGA	E20	FMC1 Vadj	
TRIGGER_0_P	Main FPGA	D19	FMC1 Vadj	
TRIGGER_0_N	Main FPGA	C19	FMC1 Vadj	
SFP_TX_P	Main FPGA	U6		AC-coupled
SFP_TX_N	Main FPGA	U5		AC-coupled
SFP_RX_P	Main FPGA	V4		AC-coupled
SFP_RX_N	Main FPGA	V3		AC-coupled
CLK_IN_P	Main PLL	In1		AC-coupled
CLK_IN_N	Main PLL	In1b		AC-coupled
SCL	Main FPGA	E9	3.3V	10k pull-up
SDA	Main FPGA	F9	3.3V	10k pull-up

Figure 5-4: High Density microHDMI Pin Assignments

5.7 MMC commands

The list of available MMC commands is shown in the following figure:

Command	Arguments	Description
? / h / help		Show list of available commands
c		Clear screen
r		Reset MMC
v		Show firmware version
xm	[0..n]	Start XMODEM update
sb		Start bootloader
vb	[0..6]	Get/Set verbosity
tm	[smart|bumb|auto]	Get/Set terminal mode
eefd		Set EEPROM factory defaults
s		Get Status
lc	[0..3] [on|off|blink] [on_ms] [off_ms]	Set LED
ser	[addr] [lun]	Get/Set event receiver
pu		Payload power up
pd		Payload power down
ppf	[stop|retry|ignore]	Get/set payload power fail policy
pc		Toggle CPLD programming / JTAG forwarding mode
sj	[con|bp|raw] [fpga(1|2|12)|rtm|fmc(1|2)]	Get/Set JTAG multiplexing
st	[0..15]	Get/Set RTM temp sensor mask
rte	[enable|override]	Get/Set RTM e-keying policy
rto	[calibrate]	Get/set I_RTM PP 12V calibration
cfu		CPLD force update
fru	[0..n]	Dump FRU information
rtp	[auto|high|low]	Get/set RTM Power Good polarity
i2cd	[ipmb|sens|rtm|pmbus|fmc1|fmc2|config|clk]	Detect I2C peripherals
i2cget	[ipmb|sens|rtm|pmbus|fmc1|fmc2|config|clk] [addr] [reg] [nbytes]	Get I2C peripheral register
i2cset	[ipmb|sens|rtm|pmbus|fmc1|fmc2|config|clk] [addr] [reg] [data]	Set I2C peripheral register
fd	[index]	Flash detect
bz	[jtag|qspi|qspi2|sd|pjtag|raw]	Get/Set ZUP boot mode
b7	[jtag|spi|spi2]	Get/Set Spartan-7 boot mode
rz		Re-configure ZUP (PS_PROG)
r7		Re-configure Spartan-7 (PROG_B)
ci	[out(0|1|2)|all] [rx19|tx19|rx20|zup|disabled|bypass]	Get/Set interlock channel(s)
vc	[low|high]	Get/Set ZUP VCC_Core
fma	[1|2|12] [8|16|auto]	Get/Set FMC1/2 EEPROM address width
fmg	[1|2|12] [enable|disable]	Enable/disable fallback for swapped GA lines
fmv	[0.95..1.9|auto]	Get/Set FMC VCC_Vadj

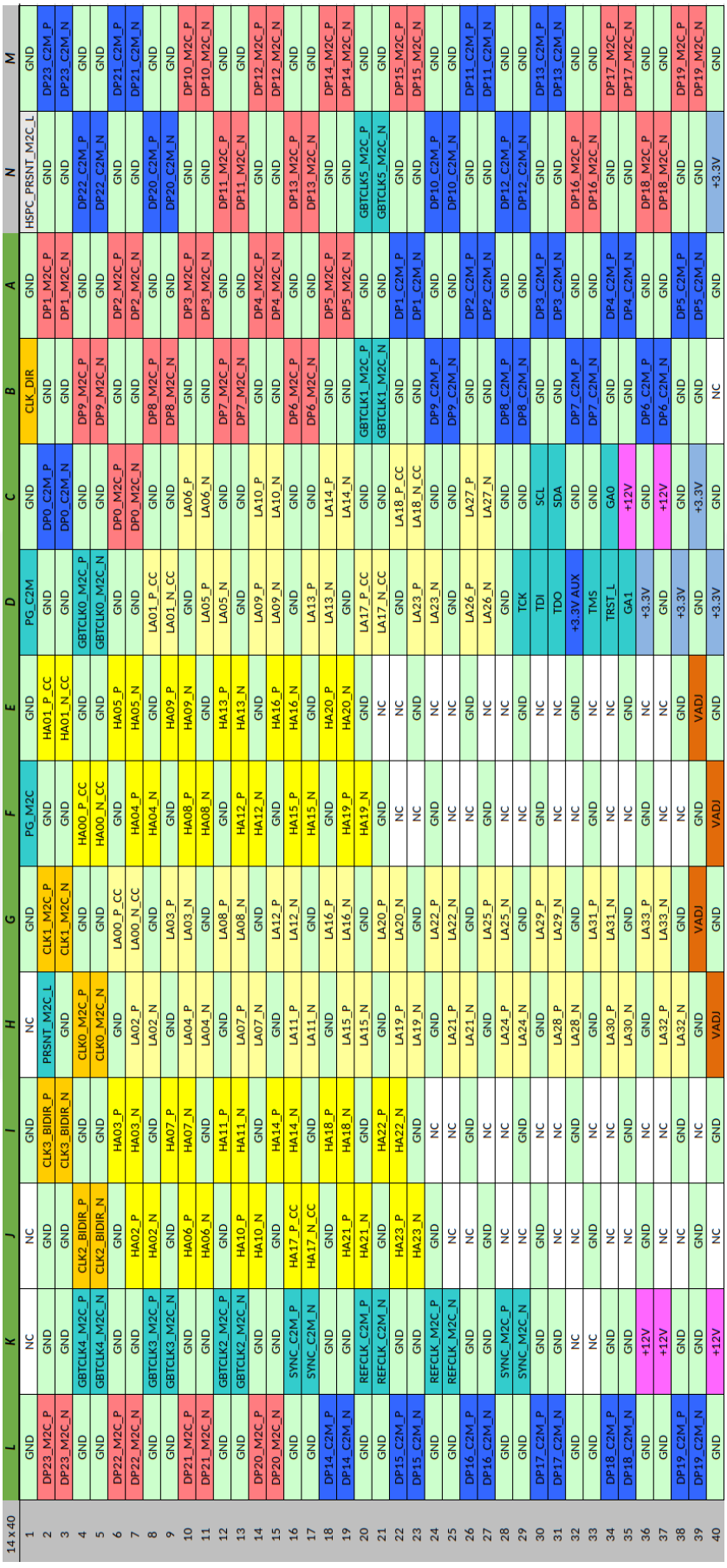
Figure 5-5: MMC Command Table

5.8 FMC/FMC+ connections

In the following figures are listed the connection to the FMC/FMC+ pins. For detailed information regarding the FMC/FMC+ assignments, please refer to the BSP (Board Support Package) project.

10 x 40	K	J	H	G	F	E	D	C	B	A
1	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	NC	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	NC	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	NC	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	NC	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	NC	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	NC	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	NC	GND	LA22_P	GND	NC	LA23_N	GND	NC	GND
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	GND
26	NC	GND	LA21_N	GND	NC	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	NC	GND	LA25_P	GND	NC	LA26_N	LA27_N	GND	DP2_C2M_N
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	GND
29	NC	GND	LA24_N	GND	NC	GND	TCK	GND	NC	GND
30	GND	NC	GND	LA29_P	GND	NC	TDI	SCL	GND	DP3_C2M_P
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	GND	DP3_C2M_N
32	NC	GND	LA28_N	GND	NC	GND	+3.3V AUX	GND	DP7_C2M_P	GND
33	GND	NC	GND	LA31_P	GND	NC	TMS	GND	DP7_C2M_N	GND
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	GND	DP4_C2M_P
35	NC	GND	LA30_N	GND	NC	GND	GA1	+12V	GND	DP4_C2M_N
36	GND	NC	GND	LA33_P	GND	NC	+3.3V	GND	DP6_C2M_P	GND
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	+12V	DP6_C2M_N	GND
38	NC	GND	LA32_N	GND	NC	GND	+3.3V	GND	GND	DP5_C2M_P
39	GND	NC	GND	VADJ	GND	VADJ	GND	+3.3V	GND	DP5_C2M_N
40	NC	GND	VADJ	GND	VADJ	GND	+3.3V	GND	NC	GND

Figure 5-6: FMC2 connections.



14 x 40	L	K	J	I	H	G	F	E	D	C	B	A	N	M
1	GND	NC	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	H5PC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	NC	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	NC	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	NC	GND	LA22_P	GND	NC	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	NC	GND	LA21_N	GND	NC	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	NC	GND	LA25_P	GND	NC	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	NC	GND	LA24_N	GND	NC	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	NC	GND	LA29_P	GND	NC	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	NC	NC	GND	LA28_N	GND	NC	GND	+3.3V AUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	NC	GND	NC	GND	LA31_P	GND	NC	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	G40	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	NC	GND	LA30_N	GND	NC	GND	GA1	+12V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	+12V	GND	NC	GND	LA33_P	GND	NC	+3.3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	+12V	NC	NC	LA32_P	LA33_N	NC	NC	GND	+12V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	NC	GND	LA32_N	GND	NC	GND	+3.3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	NC	GND	VADJ	GND	VADJ	GND	+3.3V	+3.3V	DP5_C2M_N	GND	DP19_M2C_N
40	GND	+12V	NC	GND	VADJ	GND	VADJ	GND	+3.3V	GND	NC	GND	+3.3V	GND

Figure 5-7: FMC1 connections.