FMC-Pico-1M4

4-channel 20 bit 1 MSPS FMC Floating Ammeter

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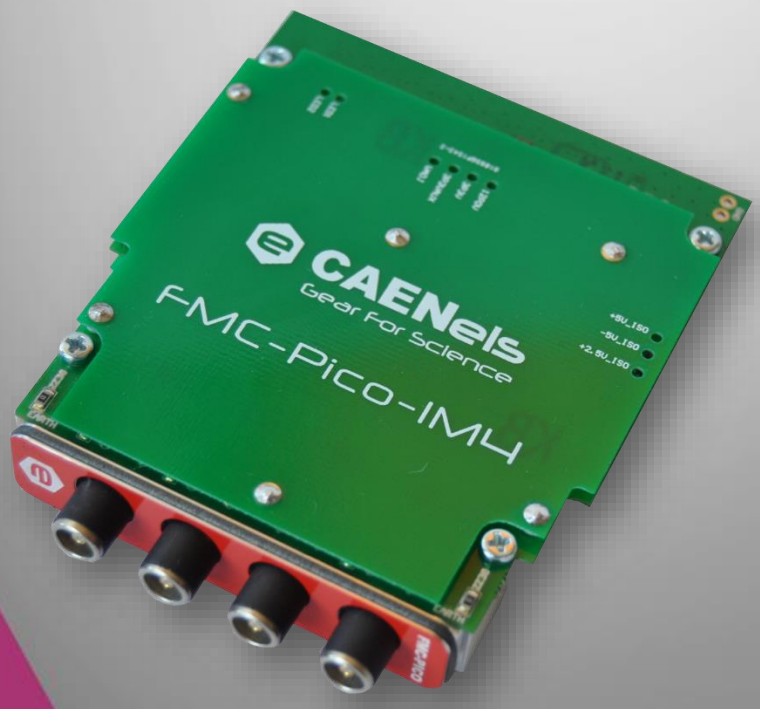
User's Manual



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FMC - FPGA MEZZANINE CARD

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Document Revisions

Document Revision	Date	Comment
1.0	November 20th, 2014	First Release
1.1	January 20th, 2015	Ordering options updated
1.2	July 21th, 2015	Photo updated, EEPROM description added
1.3	November 11th, 2018	Model FMC-PICO-1M4 and technical specifications added
1.4	March 27th, 2019	Added information on calibration parameters
1.5	July 1st, 2020	Added User Calibration Offsets (see EEPROM map)
1.6	September 17th, 2021	Added customs C4 and C5
1.7	February 14th, 2022	Added custom C6
2	August 8th 2024	Updated address and revision numbering

Safety information - Warnings

CAEN ELS will repair or replace any product within the guarantee period if the Guarantor declares that the product is defective due to workmanship or materials and has not been caused by mishandling, negligence on behalf of the User, accident or any abnormal conditions or operations.

Please read carefully the manual before operating any part of the instrument

WARNING

Do NOT open the boxes

CAEN ELS d.o.o. declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly this User's Manual before any kind of operation.

CAEN ELS d.o.o. reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.

Disposal of the Product

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.

Read over the instruction manual carefully before using the instrument.
The following precautions should be strictly observed before using the device:

WARNING

- Do not use this product in any manner not specified by the manufacturer. The protective features of this product may be impaired if it is used in a manner not specified in this manual.
- Do not use the device if it is damaged. Before you use the device, inspect the instrument for possible cracks or breaks before each use.
- Do not operate the device around explosives gas, vapor or dust.
- Always use the device with the cables provided.
- Turn off the device before establishing any connection.
- Do not operate the device with the cover removed or loosened.
- Do not install substitute parts or perform any unauthorized modification to the product.
- Return the product to the manufacturer for service and repair to ensure that safety features are maintained

CAUTION

- This instrument is designed for indoor use and in area with low condensation.

The following table shows the general environmental requirements for a correct operation of the instrument:

Environmental Conditions	Requirements
Operating Temperature	0°C to 50°C
Operating Humidity	30% to 85% RH (non-condensing)
Storage Temperature	-10°C to 60°C
Storage Humidity	5% to 90% RH (non-condensing)

This manual refers to the following boards:

- **FMCPICO1M4XA** - 4-channel 20-bit 1 MSPS FMC Dual-Range Floating Ammeter;
- **FMCPICO1M4C3** - 4-channel 20-bit 1 MSPS FMC Dual-Range Floating Ammeter (±10 mA, ±500 µA, BW=300 kHz);
- **FMCPICO1M4C4** - 4-channel 20-bit 1 MSPS FMC Dual-Range Floating Ammeter (±1 mA, ±20 uA BW=160 kHz);
- **FMCPICO1M4C5** - 4-channel 20-bit 1 MSPS FMC Dual-Range Floating Ammeter (±10 mA BW=300kHz, ±2.5 uA BW=20kHz);
- **FMCPICO1M4C6** - 4-channel 20-bit 1 MSPS FMC Dual-Range Floating Ammeter (±1 mA BW=25kHz, ±1 uA BW=25kHz);

1. Introduction

This chapter describes the general characteristics and main features of FMC-Pico-1M4 mezzanine cards.

1.1 FMC-Pico-1M4 Overview

The CAEN ELS FMC-Pico-1M4 is a standard FPGA Mezzanine Card (FMC) Low Pin Count (LPC) daughter board that allows high resolution monitoring of bipolar currents up to 1 mA (standard configuration) with maximum sampling rate of 1 MHz. It is mechanically and electrically compliant to the FMC standard (ANSI/VITA 57.1).

The front-end is composed of a specially designed trans-impedance input stage for current sensing combined with analog signal conditioning and filtering stages making use of state-of-the-art electronics. The 20-bit resolution is obtained from independent, simultaneous sampling and low-delay SAR (Successive Approximation Register) Analog to Digital Converters (ADCs).

Each channel has two full-scale measuring ranges, up to ±1 mA and ±1 µA (customizable upon request) respectively and the current source can be floating up to ±300 V respect to the FMC ground. The floating capability of the inputs is perfectly suitable for applications where the detector or current source needs to be biased.

The analog front end is designed in order to achieve low noise, low temperature dependence and very small unbalance between channels. The analog characteristics can be further improved by requesting a factory calibration of the channels. Calibration data are stored in the on-board EEPROM memory that can be read via an I2C bus on the FMC connector.

A metallic shield has a dual function of shielding the analog front end from external noise sources and also galvanically isolates the internal electronics that could be floating up to ±300 V.

A trigger signal can be fed to the FMC connector in order to start the conversion of data samples: this feature allows synchronizing the board acquisition to an external event - e.g. machining revolution frequency in storage rings.

Data readout is performed via separate SPI links - i.e. one for each channel, sharing the same clock signal.

1.2 Device Description

Both sides and the front view of the FMC-Pico-1M4 can be seen on the following **Figure 1**, **Figure 2** and **Figure 3**.

Figure 1: FMC-Pico-1M4 *side 1*

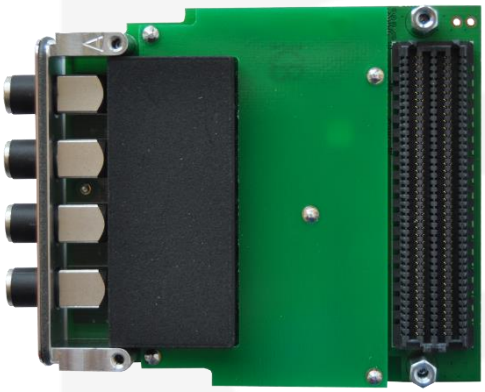

Figure 2: FMC-Pico-1M4 *side 2*

Figure 3: FMC-Pico-1M4 front view

The FMC-Pico-1M4 device is composed of the following building blocks:

- the analog front-end;
- the ADC and isolation section;
- the range selection block;
- the power supply part.

The block diagram of the whole device can be seen on the **Figure 4**.

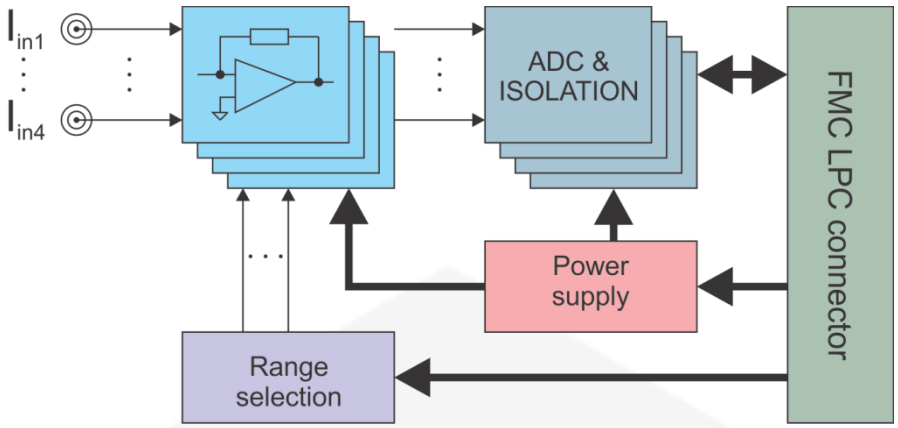

Figure 4: FMC-Pico-1M4 block diagram

The analog front end is built from several functional blocks (**Figure 5**). The current signal is fed to the device through the LEMO triaxial connector. The next stage is current-to-voltage conversion where the current signal is transformed to a voltage one and filtered. The voltage signal is then converted in a digital representation using a high performance analog-to-digital converter. Before the digital data stream reaches the FMC connector it is galvanically isolated from the analog front end. The digital voltage levels are also adapted to the FMC carrier ones.

Each analog front end has two measurement ranges which can be independently selected from channel to channel.

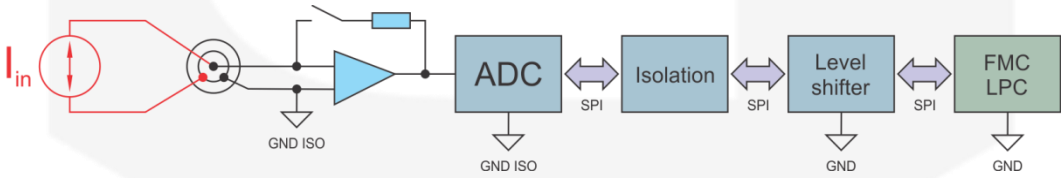

Figure 5: detailed block diagram of a single channel

The power supply part is responsible for the generation of the appropriate isolated power supply rails (+5 V, -5 V and 2.5 V), which are required for the high-quality analog-to-digital signal conversion.

There are several light emitting diodes (LEDs) on the FMC-Pico-1M4 board. The four green ones are signaling the presence of the power supply voltages that are supplied from the carrier board (12P0V, 3P3V, 3P3VAUX and VADJ).

The group of three red LEDs shows the status of power supply voltages that are generated on-board by the power supply module. The user can freely use two additional yellow LEDs upon its discretion (board status signaling, range selection, etc.).

2. Installation and Operation

The FMC-Pico-1M4 board can be installed on the FMC carrier board which is compliant to the FMC standard. The FMC-Pico-1M4 can be mounted on both low-pin count (LPC - 160 pins) and high-pin count (HPC - 400 pins) FMC connectors. Only the LPC pins are connected on the mezzanine module. The FMC carrier supports VADJ voltage range between 1.8 V and 3.3V.

During the installation and handling the ESD precautions must be respected to prevent electrostatic discharges.

2.1 Ground Connections

For safety and performance reasons the triaxial connectors are used for the measurement current inlet. The measured current path is through the center wire and the inner shield of the triaxial cable (see **Figure 6**). By convention the current that flows from the source into the FMC board through the center wire is measured as positive, on the contrary the current that is sinking by the source and flows from the FMC board through the center wire is measured as negative. The return current path is always established through the inner cable shield.

Figure 6: Measured current path

There can be large potential difference between the inner (GND ISO) and the outer triaxial cable shield (EARTH) because of the front-end isolation (**Figure 7**). The voltage between both shields must be limited as breakdown may occur so the maximum value of the isolation voltage is given in the electrical specifications section.

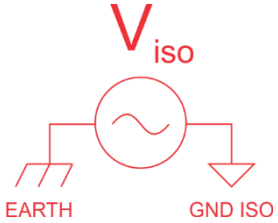

Figure 7: Definition of isolation voltage

The outer shield of the triaxial cable must be grounded. Grounding can be done in two different ways. The default way is assured by the ground connection trough the FMC bezel which is connected to the grounded chassis (see **Figure 8**).

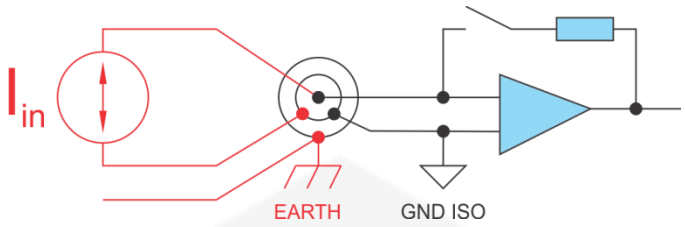

Figure 8: Grounding at the FMC bezel side

In addition it is possible also to make the ground connection using the current source side (see **Figure 9**). In this case pay attention to realize a proper grounding connection on the current source side.

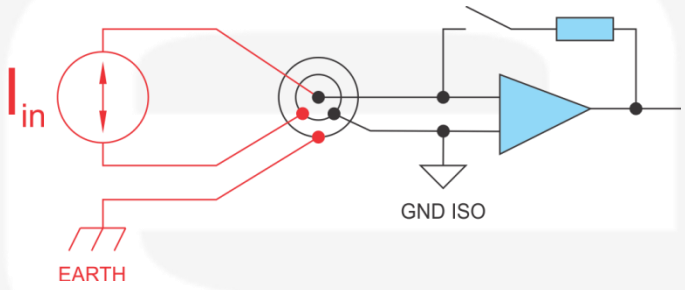

Figure 9: Grounding at the current source side

To realize the second type of connection it is necessary to unsolder the two connection jumpers on the top side of the FMC-Pico-1M4 board (see **Figure 10**).

Figure 10: Jumpers for connecting the bezel to the input connectors

2.2 Signals Definitions and Pinout

Interface signals are grouped into six categories:

- *ADC Interface*: signals which are interfacing ADCs on the FMC-Pico-1M4 board;
- *Range Selection*: signals which are used for the selection of the measurement ranges;
- *General Purpose LEDs*: driving signals for the two general purpose LEDs;
- *System Management EEPROM*: interface signals to the Module Management EEPROM, used for the IPMI standard;
- *Application EEPROM*: interface signals to the Application EEPROM memory, that can be used from the application logic;
- *Power Supply Interface*.

The definition of signal direction is as follows:

- **C2M**: carrier board sources the signal (output), mezzanine board is the signal sink (input);

- **M2C**: mezzanine board sources the signal (output), carrier board is the signal sink (input).

The LPC connector assignment of signals, its pin name and the direction, sorted by category, are presented in the following tables**.**

ADC Interface

Signal name	*LPC Pin Assignment*	*Pin Name*	*Direction*
CNV	H10	LA04_P	C2M
SCK	H11	LA04_N	C2M
SCK_RTRN	G12	LA08_P	M2C
SDO1	H17	LA11_N	M2C
SDO2	H16	LA11_P	M2C
SDO3	H14	LA07_N	M2C
SDO4	H13	LA07_P	M2C
BUSY_CMN	G13	LA08_N	M2C

Table 1: ADC interface signals

Range Selection

Signal name	*LPC Pin Assignment*	*Pin Name*	*Direction*
R1	G10	LA03_N	C2M
R2	G09	LA03_P	C2M
R3	H08	LA02_N	C2M
R4	H07	LA02_P	C2M

Table 2: Range selection signals

General Purpose LEDs

Signal name	*LPC Pin Assignment*	*Pin Name*	*Direction*
LED1	D11	LA05_P	C2M
LED2	D12	LA05_N	C2M

Table 3: General purpose LED signals

System Management EEPROM

Signal name	*LPC Pin Assignment*	*Pin Name*	*Direction*
SM_SCL	C30	SCL	C2M
SM_SDA	C31	SDA	bidirectional
SM_GA0	C34	GA0	C2M
SM_GA1	D35	GA1	C2M

Table 4: System Management EEPROM interface signals

Application EERPOM

Signal name	*LPC Pin Assignment*	*Pin Name*	*Direction*
A_SCL	D23	LA23_P	C2M
A_SDA	D24	LA23_N	bidirectional

Table 5: Application EEPROM interface signals

Power Supply Interface

Signal name	*LPC Pin Assignment*	*Pin Name*	*Direction*
VADJ	G39, H40	VADJ	C2M
3P3VAUX	D32	3P3VAUX	C2M
3P3V	C39, D36, D38, D40	3P3V	C2M
12P0V	C35, C37	12P0V	C2M

Table 6: Power supply interface signals

2.3 Signal Descriptions

- **CNV**: Convert Input. A rising edge on this input initiates a new conversion;
- **SCK**: Serial Data Clock Input. The conversion result or daisy-chain data from another ADC is shifted out on the rising edges of this clock MSB first;
- **SCK_RTRN**: Serial Data Clock Return. The return clock signal, which is used for ADC data synchronization on the FMC carrier board;
- **SDO1-4**: Serial Data Output. The conversion result or daisy-chain data is output on this pin on each rising edge of SCK MSB first. The output data is in 2's complement format;
- **BUSY_CMN**: Common BUSY Indicator. Goes high at the start of a new conversion and returns low when all the conversions have finished. BUSY signals from all four ADCs are OR-ed to make one common BUSY_CMN signal;
- **R1-R4**: Range selection signal; when the line is high, RNG0 is selected on the current channel, otherwise RNG1 is active;
- **LED1-LED2**: User LEDs control signal; when high, the corresponding LED is on;
- **SM_SCL**, **SM_SDA**, **SM_GA0** and **SM_GA1** signals are connected to the on-board Module Management EEPROM chip 24AA64. SM_SCL and SM_SDA signals are used for the I2C communication protocol; SM_GA0 and SM_GA1 are used to define the geographical address of the Module Management EEPROM;
- **A_SCL** and **A_SDA** signals are connected to the I2C bus for the communication with the on-board Application EEPROM.
- **VADJ**, **3P3VAUX**, **3P3V** and **12P0V** are the signals that provide the power supplies to the carrier board.

3. Controlling the FMC

3.1 Digital Interface

The ADCs simultaneous conversion is controlled by CNV signal. A rising edge on CNV will starts the conversion of the 4 input channels. Once a conversion has been initiated, it cannot be restarted until the conversion is completed. For optimum performance, CNV should be driven by a clean low jitter signal. Conversion status is indicated by the BUSY output which remains high while the conversions are in progress. To ensure that no errors occur in the digitized results, any additional transitions on CNV should occur within 40 ns from the start of the conversion or after the conversion has been completed. Once the conversion has completed, the ADCs begin acquiring the input signal.

The ADCs have an internal clock that is trimmed to achieve a maximum conversion time of 675 ns. With a minimum acquisition time of 312 ns, throughput performance of 1Msps is guaranteed.

The ADCs transmit the acquired data using a serial digital interface. The ADCs are galvanically isolated from the FMC connector. The isolation logic introduce some delay on the SPI signals. The serial clock signal (SCK) is brought back through the isolation (SCK_RTRN signal) in order to have a signal aligned with the SDO data outputs (see **Figure 11**). For this reason, all the reads of the SDO lines, have to be based on the edges of the SCK_RTRN signal.

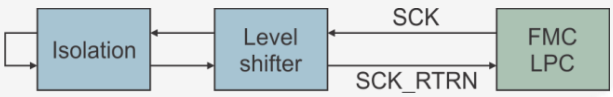

Figure 11: Clock loopback block diagram

The serial output data are clocked out on the SDO pins when an external clock is applied to the SCK pin. With a shift clock frequency of at least 64MHz (the max shift clock frequency is 100 MHz), a 1MSps throughput is still achieved. The serial output data changes state on the rising edge of the isolated SCK. The SDO lines have to be read simultaneously from the FMC carrier logic (see **Figure 12**).

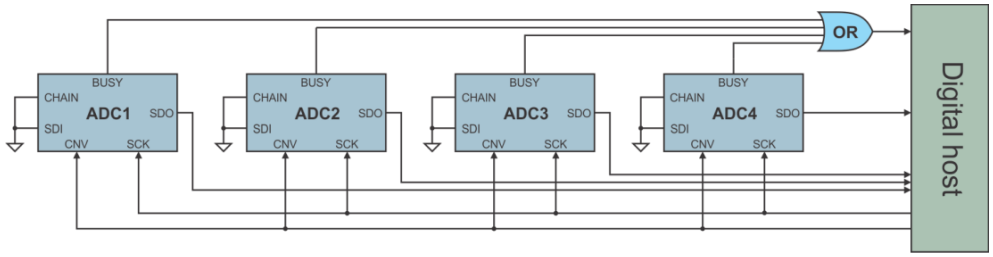

Figure 12: Parallel connection of the SDO lines

3.2 Timing Diagrams

The SDO signal is always driven. MSB (D19) of the new conversion data is available at the falling edge of BUSY signal. This is the simplest way to operate the four ADCs. The timing diagram is shown in **Figure 13**.

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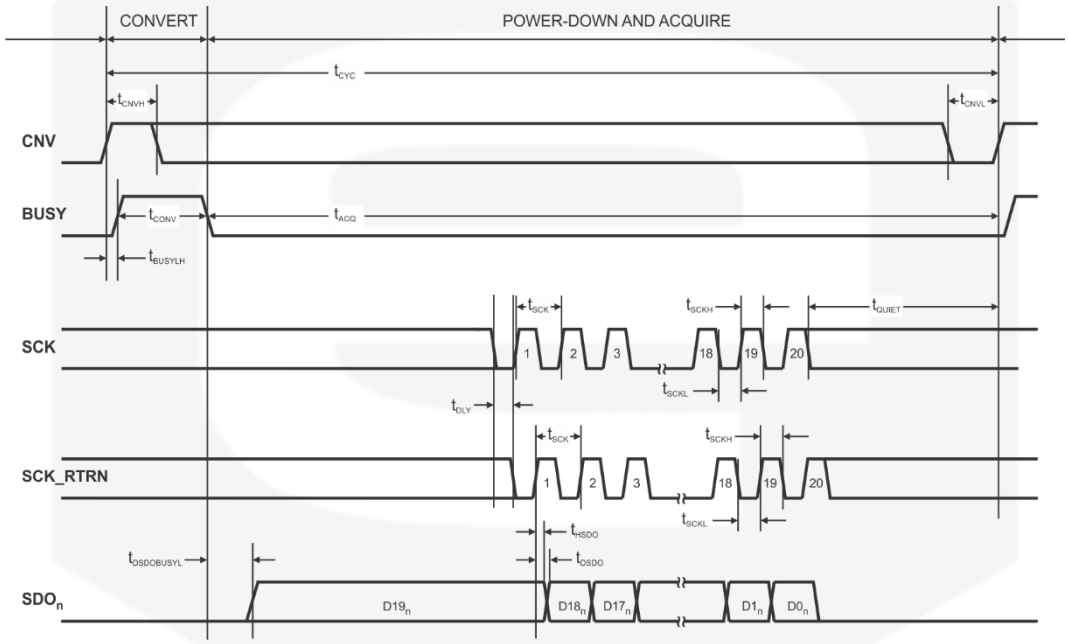

Figure 13: Timing diagram

3.3 Timing Characteristics

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*
f_{SMPL}	Maximum Sampling Frequency			1	Msps
t_{CONV}	Conversion Time	615		675	ns
t_{ACQ}	Acquisition Time	286			ns
t_{CYC}	Time Between Conversions	1			µs
t_{CNVH}	CNV High Time	20			ns
t_{BUSYLH}	CNV↑ to BUSY Delay		25	39	ns
t_{CNVL}	Minimum Low Time for CNV	20			ns
t_{QUIET}	SCK Quiet Time from CNV↑	15			ns
t_{SCK}	SCK Period	10			ns
t_{SCKH}	SCK High Time	4			ns
t_{SCKL}	SCK Low Time	4			ns
$t_{SSDISCK}$	SDI Setup Time From SCK↑	4			ns
$t_{HSDISCK}$	SDI Hold Time From SCK↑	1			ns
t_{SCKCH}	SCK Period in Chain Mode	13.5			ns
t_{DSDO}	SDO Data Valid Delay from SCK_RTRN↑			10.5	ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK_RTRN↑	-1.5			ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓			7.5	ns
t_{DLY}	SCK to SCK_RTRN delay	10	16	28	ns

Table 7: Timing characteristics

3.4 EEPROM Interfaces

The FMC-Pico-1M4 carries two serial EEPROM chips (Microchip 24AA64) with the same content and connected to two separated I2C interfaces:

- **System Management EEPROM**: accessible using the reserved IPMI interface (standard ANSI/VITA 57.1), for the management purposes;
- **Application EEPROM**: accessible through I2C interface on the FMC connector, for application purposes.

The address of the of the System Management EEPROM is configured using the Geographical Addresses GA0 and GA1 as defined in the FMC standard ANSI/VITA 57.1. The address pins of the Application EEPROM are fixed to a low level, which set the address of this memory to **0b1010000** (0x50).

The content of both EEPROMs is the same, allowing user a flexible access to calibration data both from FMC management logic and application logic. The content of the memory is compliant with Intel IPMI Platform Management FRU Information Storage Definition v1.0 standard.

As defined in the standard, the Board Info Area presents the following information:

```
Date of Man      : Wed Jun 10 01:00:00 2015
Manufacturer     : CAEN ELS d.o.o.
Product Name     : FMC-Pico-1M4
Serial Number    : 15001
Part Number      : FMCPICO1M420
```

Figure 14: EEPROM Board Info Area

The Multi Record Area presents the power supply information as defined in the FMC standard:

```
DC Load
  Output number: 0 (P1 VADJ)
  Nominal Volts:         2500 (mV)
  minimum voltage:       1800 (mV)
  maximum voltage:       3300 (mV)
  Ripple and Noise pk-pk 0000 (mV)
  Minimum current load   0000 (mA)
  Maximum current load   0100 (mA)
DC Load
  Output number: 1 (P1 3P3V)
  Nominal Volts:         3300 (mV)
  minimum voltage:       3120 (mV)
  maximum voltage:       3460 (mV)
  Ripple and Noise pk-pk 0000 (mV)
  Minimum current load   0000 (mA)
  Maximum current load   0100 (mA)
DC Load
  Output number: 2 (P1 12P0V)
  Nominal Volts:         12000 (mV)
  minimum voltage:       11400 (mV)
  maximum voltage:       12600 (mV)
```

```
  Ripple and Noise pk-pk 0000 (mV)
  Minimum current load   0000 (mA)
  Maximum current load   0300 (mA)
DC Output
  Output Number: 3 (P1 VIO_B_M2C)
  All Zeros
DC Output
  Output Number: 4 (P1 VREF_A_M2C)
  All Zeros
DC Output
  Output Number: 5 (P1 VREF_B_M2C)
  All Zeros
```

Figure 15: EEPROM Multi Record Area

The Internal Use Area saves the calibration data. This area always starts at the address 0xC8, with data starting at 0xCD (there is a 5 byte header as defined in IPMI standard). The memory is organized in fields of 32 bits (4 bytes) with **little-endian** data encoding. The complete Internal Use Area is shown in the following table:

Absolute address	*Field Description*	*Example*
0xCD	Magic number 0 (0xCAE2E150)	50 e1 e2 ca
0xD1	Magic number 1 (0xF22C71C0)	c0 71 2c f2
0xD5	RNG #0, CH #0 Gain (IEEE754 float)	90 e4 04 31
0xD9	RNG #0, CH #0 Offset (IEEE754 float)	bd 89 98 32
0xDD	RNG #0, CH #1 Gain (IEEE754 float)	ea e1 04 31
0xE1	RNG #0, CH #1 Offset (IEEE754 float)	d4 65 50 b3
0xE5	RNG #0, CH #2 Gain (IEEE754 float)	4b e1 04 31
0xE9	RNG #0, CH #2 Offset (IEEE754 float)	fc 50 0c 32
0xED	RNG #0, CH #3 Gain (IEEE754 float)	9d e1 04 31
0xF1	RNG #0, CH #3 Offset (IEEE754 float)	7f d1 cd b2
0xF5	RNG #1, CH #0 Gain (IEEE754 float)	47 72 0c 2c
0xF9	RNG #1, CH #0 Offset (IEEE754 float)	4d be b0 2c
0xFD	RNG #1, CH #1 Gain (IEEE754 float)	f4 6d 0c 2c
0x101	RNG #1, CH #1 Offset (IEEE754 float)	85 54 87 ae
0x105	RNG #1, CH #2 Gain (IEEE754 float)	f3 6d 0c 2c
0x109	RNG #1, CH #2 Offset (IEEE754 float)	1e a2 81 ac
0x10D	RNG #1, CH #3 Gain (IEEE754 float)	1b 71 0c 2c
0x111	RNG #1, CH #3 Offset (IEEE754 float)	c3 3d 14 ae
0x115	Calibration timestamp (UNIX time)	c8 84 af 55
0x119	Hardware revision (2.1)	01 02 00 00
0x11D	Magic number 3 (0x25ECA11B)	1b a1 ec 25
0x121	RNG #0, CH #0 User Offset (IEEE754 float)	d5 b2 d9 ab
0x125	RNG #1, CH #0 User Offset (IEEE754 float)	3f 4e 66 2e
0x129	RNG #0, CH #1 User Offset (IEEE754 float)	dc 93 06 2d
0x12D	RNG #1, CH #1 User Offset (IEEE754 float)	fc 49 db 2c
0x131	RNG #0, CH #2 User Offset (IEEE754 float)	da c2 db ab
0x135	RNG #1, CH #2 User Offset (IEEE754 float)	f6 f0 3b 2e
0x139	RNG #0, CH #3 User Offset (IEEE754 float)	e0 2f ba ab
0x13D	RNG #1, CH #3 User Offset (IEEE754 float)	bb 3e d2 2d

Table 8: EEPROM Internal Use Area

An example dump of the EEPROM memory is the following:

```
00000000 01 19 00 01 00 09 00 dc 01 08 00 80 01 9c cf 43 |...............C|
00000010 41 45 4e 20 45 4c 53 20 64 2e 6f 2e 6f 2e cc 46 |AEN ELS d.o.o..F|
00000020 4d 43 2d 50 69 63 6f 2d 31 4d 34 c5 31 35 30 30 |MC-Pico-1M4.1500|
00000030 31 cc 46 4d 43 50 49 43 4f 31 4d 34 32 30 c0 c1 |1.FMCPICO1M420..|
00000040 00 00 00 00 00 00 00 ad 02 02 0d b5 3a 02 b0 04 |............:...|
00000050 74 04 ec 04 00 00 00 00 2c 01 02 02 0d bc 33 01 |t.......,.....3.|
00000060 4a 01 38 01 5a 01 00 00 00 00 64 00 02 02 0d a3 |J.8.Z.....d.....|
00000070 4c 00 fa 00 b4 00 4a 01 00 00 00 00 64 00 01 02 |L.....J.....d...|
00000080 0d fb f5 05 00 00 00 00 00 00 00 00 00 00 00 00 |................|
00000090 01 02 0d fc f4 04 00 00 00 00 00 00 00 00 00 00 |................|
000000a0 00 00 01 02 0d fd f3 03 00 00 00 00 00 00 00 00 |................|
000000b0 00 00 00 00 fa 82 0b 08 71 a2 12 00 00 00 44 00 |........q.....D.|
000000c0 00 00 00 00 00 00 00 00 01 50 00 00 00 50 e1 e2 |.........P...P..|
000000d0 ca c0 71 2c f2 90 e4 04 31 bd 89 98 32 ea e1 04 |..q,....1...2...|
000000e0 31 d4 65 50 b3 4b e1 04 31 fc 50 0c 32 9d e1 04 |1.eP.K..1.P.2...|
000000f0 31 7f d1 cd b2 47 72 0c 2c 4d be b0 2c f4 6d 0c |1....Gr.,M..,.m.|
00000100 2c 85 54 87 ae f3 6d 0c 2c 1e a2 81 ac 1b 71 0c |,.T...m.,.....q.|
00000110 2c c3 3d 14 ae c8 84 af 55 01 02 00 00 1b a1 ec |,.=.....U.......|
00000120 25 d5 b2 d9 ab 3f 4e 66 2e dc 93 06 2d fc 49 db |%...?Nf....-.I.,|
00000130 2c da c2 db ab f6 f0 3b 2e e0 2f ba ab bb 3e d2 |,......;../...>.|
00000140 2d 0a                                          |-.              |
```

Figure 16: EEPROM memory content

A more detailed description of the EEPROMs and their timing diagrams can be found in the manufacturer datasheet (Microchip 24AA64).

3.4.1 Purpose of Calibration Parameters

As described in Table 8, for each channel in the FMC-Pico-1M4 board, three calibration parameters are stored in the EEPROM, said "Offset, "Gain" and "User Offset". "User offset" parameters are set to 0 by factory. "User offset" parameters are

applied at startup only if the "Magic number 3" is present at offset 0x11D of the eeprom.

These parameters are used to convert the current value read by the board (ADC count, said "readvalue"), to the actual current value (said "actualcurrentvalue").

To do so, the user must apply the following formula:

$$actualcurrentvalue = (Offset + Gain * readvalue) + UserOffset$$

3.5 CAENels AMC-PICO-8

The FMC-Pico-M4 can be installed on the DAMC-FMC25 MTCA.4 carrier board produced by CAEN ELS (see **Figure 17**). This solution is called **AMC-PICO-8**. Up to two FMC cards can be installed on a single carrier, allowing to configure an 8-channel current-measuring board. Please note that the input channels of one FMC board can be at a different potential respect to the input channels of the other FMC board installed. Since the input channels of one FMC board can float up to ±300 V respect to ground, the maximum potential difference between the input channels of one FMC board and the other can be of 600 V. For more detailed information, please visit our webpage or contact us directly.

Figure 17: CAENels AMC-PICO-8

4. Ordering Options

4.1 Ordering Codes

Customization and calibration of the input ranges of the FMC-Pico-1M4 can be optionally performed upon request.

The **FMC-Pico-1M4** unit has several options available, listed below:

Ordering Code	Ranges	BW
FMCPICO1M4XA	± 1 mA ± 1 µA	10 kHz
FMCPICO1M4C3	± 10 mA ± 500 µA	300 kHz
FMCPICO1M4C4	± 1 mA ± 20 µA	200 kHz 170 kHz
FMCPICO1M4C5	± 10 mA ± 2.5 µA	300 kHz 20 kHz
FMCPICO1M4C6	± 1 mA ± 1 µA	25 kHz

5. Technical Specifications

Technical Specifications for the FMC-PICO-1M4 mezzanine cards (also the FMC-PICO-1M4-C3 version) are hereafter presented:

General Technical Specifications	
Board Type	FPGA Mezzanine Card - FMC VITA 57.1
FMC Connector Type	LPC (HPC compliant)
Number of Channels	4
On Board Input Connectors	Triaxial - LEMO 00.650 Series (EPL.00.650)

Table 9: General information for the FMC-Pico-1M4

5.1 Electrical Specifications

The electrical specifications for the FMC-PICO-1M4 are the following:

Electrical Specifications – **FMC-PICO-1M4**	
Current Polarity	Bipolar
Full-Scale Current	RNG0: ± 1 mA RNG1: ± 1 µA
Maximum Sampling Rate	1 MSPS
Equivalent Signal-to-Noise	RNG0: > 100 dB RNG1: > 90 dB
Resolution	20 bit
Conversion Time - T_{CONV}	650 ns
Bandwidth (-3dB)	> 10 kHz
Temperature Coefficient - TC	10 ppm/°C
Differential TC	< 25 ppm/°C
Front End Isolation Voltage	± 300 V

Table 10: Electrical specifications for FMC-Pico-1M4

The electrical specifications for the FMC-PICO-1M4-C3 are the following:

***Electrical Specifications* – FMC-PICO-1M4-C3**	
Current Polarity	Bipolar
Full-Scale Current	RNG0: ± 10 mA RNG1: ± 500 µA
Maximum Sampling Rate	1 MSPS
Equivalent Input Noise	RNG0: < 230 nA_{RMS} RNG1: > 15 nA_{RMS}
Resolution	20 bit
Conversion Time - T_{CONV}	650 ns
Bandwidth (-3dB)	300 kHz ± 10 %
Temperature Coefficient - TC	50 ppm/°C
Differential TC	< 25 ppm/°C
Front End Isolation Voltage	± 300 V

Table 11: Electrical specifications for FMC-Pico-1M4-C3

The electrical specifications for the FMC-PICO-1M4-C4 are the following:

***Electrical Specifications* – FMC-PICO-1M4-C4**	
Current Polarity	Bipolar
Full-Scale Current	RNG0: ± 1 mA RNG1: ± 20 µA
Maximum Sampling Rate	1 MSPS
Equivalent Input Noise	RNG0: < 25 nA_{RMS} RNG1: < 1.2 nA_{RMS}
Resolution	20 bit
Conversion Time - T_{CONV}	650 ns
Bandwidth (-3dB)	RNG0: 200 kHz ± 10 % RNG1: 170 kHz ± 10 %
Temperature Coefficient - TC	50 ppm/°C
Differential TC	< 25 ppm/°C
Front End Isolation Voltage	± 300 V

Table 12: Electrical specifications for FMC-Pico-1M4-C4

The electrical specifications for the FMC-PICO-1M4-C5 are the following:

***Electrical Specifications* – FMC-PICO-1M4-C5**	
Current Polarity	Bipolar
Full-Scale Current	RNG0: ± 10 mA RNG1: ± 2.5 µA
Maximum Sampling Rate	1 MSPS
Equivalent Input Noise	RNG0: < 230 nA_{RMS} RNG1: < 290 pA_{RMS}
Resolution	20 bit
Conversion Time - T_{CONV}	650 ns
Bandwidth (-3dB)	RNG0: 300 kHz ± 10 % RNG1: 20 kHz ± 10 %
Temperature Coefficient - TC	50 ppm/°C
Differential TC	< 25 ppm/°C
Front End Isolation Voltage	± 300 V

Table 13: Electrical specifications for FMC-Pico-1M4-C5

The electrical specifications for the FMC-PICO-1M4-C6 are the following:

***Electrical Specifications* – FMC-PICO-1M4-C6**	
Current Polarity	Bipolar
Full-Scale Current	RNG0: ± 1 mA RNG1: ± 1 µA
Maximum Sampling Rate	1 MSPS
Equivalent Input Noise	RNG0: < 15 nA_{RMS} RNG1: < 25 pA_{RMS}
Resolution	20 bit
Conversion Time - T_{CONV}	650 ns
Bandwidth (-3dB)	RNG0: 25 kHz ± 10 % RNG1: 25 kHz ± 10 %
Temperature Coefficient - TC	50 ppm/°C
Differential TC	< 25 ppm/°C
Front End Isolation Voltage	± 300 V

Table 14: Electrical specifications for FMC-Pico-1M4-C5

5.2 Equivalent Input Noise

Different equivalent input noise typical values for the two standard different measuring ranges and for different sampling rates are hereafter presented.

Noise tests are performed by shorting the signal ground on the chassis ground and by shielding the inputs.

Equivalent Input Noise		
	RNG0: ±1 mA	**RNG1: ±1 µA**
F_S = 2 ksps	1 ppm/FS **-120 dB**	2.5 ppm/FS **-112 dB**
F_S = 20 ksps	2 ppm/FS **-114 dB**	7 ppm/FS **-103 dB**
F_S = 200 ksps	5 ppm/FS **-107 dB**	10 ppm/FS **-100 dB**
F_S = 1 Msps	8 ppm/FS **-102 dB**	15 ppm/FS **-96 dB**

Table 15: Equivalent Input noise for different sampling rates of the FMC-PICO-1M4

The basic sampling rate is 1 Msps and the computation is made by averaging the number of samples in order to reach the other listed values – e.g. averaging of 5 samples to obtain the F_S = 200 ksps equivalent input noise value.

5.3 Digital Interface and Power Supply Requirements

The FMC-Pico-1M4 is designed to operate in the LVCMOS mode from 1.8 V to 3.3 V, depending on the voltage supply level provided by the carrier board on the VADJ pins. VREF_A_M2C pin is unconnected on the mezzanine module.

The current consumption for all four power supply voltages is indicated in the **Table 16**. To prevent overheating of the FMC board the user must ensure appropriate airflow.

Power Supply Voltage	*Allowed Voltage Range [V]*	*Number of Pins*	*Max Current Consumption*	*Tolerance*
VADJ	**1.2 – 3.3**	2	10 mA @ 2.5 V	±5 %
3P3VAUX	**3.3**	1	5 mA	±5 %
3P3V	**3.3**	4	25 mA	±5 %
12P0V	**12**	2	150 mA	±5 %

Table 16: Current consumption for all power supply voltages

6. Mechanical Dimensions

The FMC-Pico-1M4 board complies with the FMC standard known as ANSI/VITA 57.1. The board is a single-width, air cooled FMC card with front panel I/O connectors and used region 1. The stacking height of the FMC-Pico-1M4 is 10 mm.

There are four LEMO triaxial connectors (EPL.00.650) available on the front panel. The user must use appropriate mating connectors to meet electrical specifications (e.g. LEMO FFC.00.65). The channel numbering is shown on **Figure 18**.

Figure 18: Front Panel Layout

The mechanical dimensions of the FMC board can be found in the following table.

Dimension	*Value*
FMC Form Factor	Single-width
Physical Width	69 mm
Physical Depth (including bezel)	78.5 mm

Table 17: Mechanical dimensions